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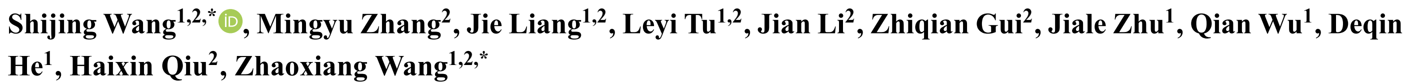
Article

Realization and optimization of super-junction structures for high-efficiency silicon carbide power devices



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Abstract: In this study, various silicon carbide (SiC) trench and via pattern etching processes are investigated, and high-aspect-ratio super-junction (SJ) structures are successfully fabricated. SiC SJ trenches are promising for ultra-high-voltage power device applications. Using a SiO_2 hard mask, SiC trenches with aspect ratios from 3:1 to 15:1 and depths exceeding 21 μm are prepared. Etch selectivity (SiC/SiO_2) is calculated based on the etched thicknesses of SiC and SiO_2 under the same process, and the selectivity can exceed 10:1 by optimizing hardware configuration and process parameters, especially gas combination and equipment settings. The significant effect of sidewall roughness transfers from the oxide hard mask to the SiC substrate is revealed. A smooth and optimized oxide hard mask sidewall is the key to reducing the final SiC sidewall roughness during pattern transfer. Full-wafer uniformity is improved by multiple tuning methods, including power ratio split, gas ratio split, temperature distribution control, and refined process parameters. Excellent uniformity is achieved: SiC trench critical dimension (CD) variation below 2%, SiC etch depth uniformity below 1%, and sidewall angles above 88° across the entire wafer. Long-term tool stability is verified over 10 consecutive months of etch rate monitoring with standard monitor wafers. The etch rate variation is controlled within 3% and uniformity below 2%, demonstrating reliable mass-production manufacturability of the SiC trench process.

Keywords: silicon carbide; super-junction trench; high-aspect-ratio; etch selectivity; side wall profile

1. Introduction

Driven by the global energy transition and the growing demand for high-efficiency power electronic systems, modern power grids and power electronic devices are evolving toward higher operating voltages, power densities, and energy efficiencies, which imposes stringent performance requirements on semiconductor components. Traditional silicon (Si) materials have gradually reached their inherent performance limits in ultra-high-voltage and high-power applications, constrained by their fundamental bandgap, breakdown electric field, and thermal conductivity characteristics [1–5]. Therefore, semiconductor materials with lower on-state resistance, higher breakdown field strength, and superior thermal performance are urgently required to advance next-generation power electronics.

As a prevailing third-generation wide-bandgap semiconductor material, silicon

carbide (SiC) possesses superior physicochemical properties and has emerged as a promising candidate for high-performance next-generation power devices [6–10]. In particular, 4H-SiC features a bandgap of approximately 3.26 eV, a critical breakdown field of ~2.8 MV/cm, and a thermal conductivity of up to 490 W/(m·K) [11–15], enabling robust operational performance under high-temperature, high-frequency, and high-voltage conditions [16–18]. The adoption of SiC power devices effectively reduces system power loss, improves energy conversion efficiency, and facilitates the achievement of global carbon peaking and carbon neutrality targets [19, 20]. Consequently, SiC devices exhibit irreplaceable application value and broad market prospects in new energy vehicles, high-speed railways, smart power grids, and aerospace systems.

Existing studies have predominantly focused on the fundamental material characteristics and conventional etching processes of SiC. Nevertheless, systematic investigations on high-aspect-ratio super-junction trench etching with ultra-smooth sidewalls, satisfactory full-wafer uniformity, and reliable long-term manufacturability remain insufficient. Trench etching and patterning are pivotal manufacturing processes that directly determine the electrical performance and production yield of SiC devices. Specifically, SiC trench morphology strongly affects device on-resistance and breakdown voltage: smooth trench sidewalls minimize conduction resistance, while rounded bottom corners mitigate electric field aggregation and enhance breakdown field strength [21–25]. Owing to the extreme hardness, excellent chemical inertness, and robust Si–C covalent bonds (~446 kJ/mol) of SiC [26, 27], conventional wet etching techniques suffer from low efficiency and poor patterning capability, making plasma-based dry etching the dominant industrial solution. However, high-density plasma excitation and energetic ion bombardment during dry etching inevitably induce surface damage, sidewall roughness, and profile distortion. For ultra-high-voltage SiC devices requiring deep trenches (depth > 20 μm) and high aspect ratios (>10:1), critical challenges including aspect ratio dependent etching (ARDE), roughness transfer, and bottom profile distortion severely degrade device breakdown performance and operational reliability [28,29].

In ultra-high-voltage SiC power devices, the super-junction (SJ) structure serves as a core technology to break the fundamental “silicon limit” and fully leverage the inherent performance advantages of SiC materials. The SJ structure realizes charge balance via alternately arranged P-type and N-type vertical drift pillars, which substantially reduces device on-resistance while maintaining a high breakdown voltage. This design effectively resolves the inherent trade-off between breakdown voltage and on-resistance in conventional power devices [28,30]. However, high-quality fabrication of SiC SJ trenches demands high aspect ratios, vertically aligned profiles, ultra-smooth sidewalls, controllable bottom morphology, as well as excellent batch-to-batch uniformity and long-term process stability. The absence of mature high-aspect-ratio deep trench etching technology has become a critical bottleneck restricting the industrialization of high-performance SiC SJ devices.

Etching equipment performance is another decisive factor governing SiC trench fabrication quality. High-precision deep trench etching requires rigorous

plasma regulation, including dual-frequency radio frequency (RF) power modulation, multi-channel gas flow control, wide-range pressure and temperature tuning, and uniform wafer thermal management. Additionally, chamber anti-contamination design, large-diameter wafer processing uniformity, and long-term operational stability directly affect device production yield and manufacturing cost. In this work, systematic investigations on the patterning and process optimization of SiC trench and via structures are conducted, with a particular focus on the fabrication mechanism and parameter optimization of high-aspect-ratio SJ structures. Key process challenges, including sidewall roughness transfer and full-wafer uniformity deviation, are comprehensively analyzed. Furthermore, 10-month continuous process monitoring verifies the long-term stability and mass manufacturability of the developed process. Through optimized etching equipment configuration and process parameter tuning, high-aspect-ratio SiC trenches featuring vertical smooth sidewalls and rounded bottom corners are successfully fabricated. This work provides critical technical support for the industrial production of ultra-high-voltage, high-efficiency SiC SJ power devices.

This study has certain limitations. The proposed process is developed based on 8-inch 4H-SiC substrates using a custom-built inductively coupled plasma (ICP) etcher. The process compatibility with alternative chamber materials and different wafer sizes (smaller or larger than 8 inches) requires further validation. Moreover, the ultra-long-term process stability beyond 10 months and operational robustness under extreme mass production conditions remain to be systematically evaluated.

2. Materials and methods

2.1. Experimental materials

Commercial 8-inch n-type 4H-SiC single-crystal substrates with a thickness of 350 μm and a (001) crystal orientation were employed in all experiments. Prior to fabrication, all SiC substrates underwent standard chemical mechanical polishing (CMP) to achieve an ultra-smooth surface with an average surface roughness (Ra) below 1 nm, which is essential for high-quality subsequent thin-film deposition and precision etching. Substrates were cleaned via standard wet cleaning procedures to eliminate surface organic residues, metal impurities, and microparticles, followed by drying with high-purity nitrogen gas.

A 1–6 μm-thick silicon dioxide (SiO_2) hard mask was deposited via plasma-enhanced chemical vapor deposition (PECVD) at a substrate temperature of approximately 300 °C. A 2–5 μm photoresist (PR) layer was subsequently spin-coated on the SiO_2 film with optimized parameters: 3,000–5,000 rpm, 30–60 s, and 0.5–3 mL dispensing volume. Target patterned structures were obtained after photolithographic exposure and development. For comparative analysis, nickel (Ni) metal masks were fabricated via magnetron sputtering under chamber pressures of 3–10 mTorr, sputtering powers of 100–300 W, and deposition durations of 5–20 min. The etching selectivity and pattern transfer accuracy of Ni metal masks and SiO_2 hard masks were systematically compared.

2.2. Etching equipment and process parameters

All SiC etching experiments with aspect ratios ranging from 1:1 to 15:1 were performed using a Bangxin Honghu Ivory150SCE/200SCE ICP etcher. The equipment is equipped with a dual-frequency RF power system: the upper 13.56 MHz ICP RF source generates high-density reactive plasma, while the lower bias RF source (switchable at 13.56 MHz or 400 kHz) precisely regulates ion bombardment energy. The two independent RF systems enable flexible and decoupled modulation of plasma density and incident ion energy. The inner chamber wall is coated with yttrium oxide (Y_2O_3) ceramic, which exhibits excellent corrosion resistance to fluorine-based and chlorine-based plasmas. This specialized coating effectively suppresses particulate and metal contamination and improves long-term process stability.

A high-precision multi-channel gas mass flow controller was integrated to precisely regulate the flow rates of process gases, including SF_6, O_2, Ar, SiF_4, Cl_2, He, N_2 and HBr. Among these precursors, SiF_4, Cl_2 and HBr serve as critical reactive gases for high-aspect-ratio SiC trench etching. The etcher supports a wide process window, with a chamber pressure ranging from 5 mTorr to 10 Torr and a wafer temperature adjustable from −20 °C to 80 °C via an electrostatic chuck (ESC) chiller and a helium backside cooling system. The electrode spacing was fixed throughout all deep trench etching experiments. All of the aforementioned parameters are critical for optimizing the cross-sectional profile of high-aspect-ratio SiC trenches.

2.3. Characterization and testing methods

Comprehensive morphological and dimensional characterizations were conducted on etched SiC samples using multiple precision testing instruments, with detailed characterization methods described as follows:

(1) Field-emission scanning electron microscopy (FESEM, Hitachi SU8600): Used to characterize the cross-sectional and surface morphology of etched trenches and measure key dimensional parameters, including trench depth, critical dimension (CD), sidewall inclination angle, and bottom profile.

(2) Transmission electron microscopy (TEM, JEOL JEM-2100F): Adopted to analyze high-resolution cross-sectional microstructure and surface elemental composition of SiC trenches.

(3) Atomic force microscopy (AFM, Bruker Dimension Icon): Employed in tapping mode with a 10 μm × 10 μm scanning area to quantitatively evaluate trench sidewall roughness, including root-mean-square (RMS) and Ra values.

(4) Optical emission spectroscopy (OES): Applied for real-time in-situ plasma state monitoring and precise etching endpoint detection.

The average etching rate was calculated as the ratio of trench depth to effective etching duration. The SiC/SiO_2 etching selectivity was defined as the quotient of the SiC etching rate and the SiO_2 hard mask etching rate. Full-wafer fabrication uniformity was evaluated by measuring trench CD and etching depth at five representative positions (wafer center and four edge locations) on 8-inch substrates. Long-term process stability was verified via 10 consecutive months of monitoring using standard

monitor wafers to validate mass-production feasibility.

3. Results and discussion

Figure 1 illustrates the typical trench and via structures fabricated on SiC power devices, covering gate trenches, front-side vias, back-side vias, Zero Mark (ZM) shallow trenches, terminal edge structures, and SJ deep trenches. Each structure possesses unique structural characteristics and corresponding etching process requirements to satisfy distinct device functional demands.

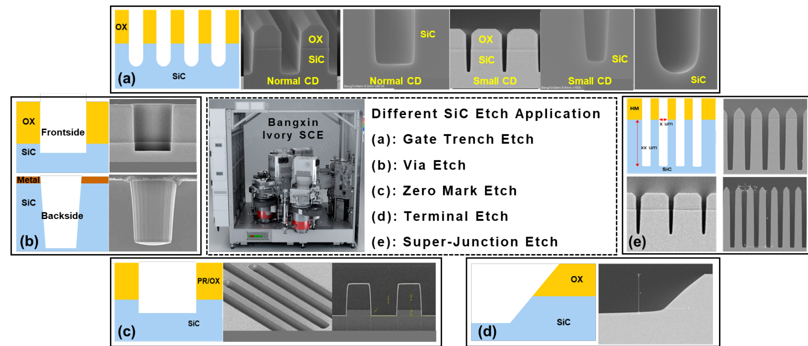

Figure 1. Typical SiC etching structures for power devices: **(a)** Gate trench; **(b)** Front-side and back-side via; **(c)** ZM shallow trench; **(d)** Terminal structure; **(e)** SJ deep trench.

In SiC metal-oxide-semiconductor field-effect transistors (MOSFETs), gate trench morphology dominates channel electrical characteristics and device switching performance. A high-quality gate trench requires a sidewall angle greater than 88.5°, sidewall roughness (Ra) lower than 1 nm, and smooth rounded bottom corners. Vertically aligned sidewalls facilitate uniform gate oxide layer deposition; ultra-smooth sidewall surfaces reduce interface trap density and leakage current, thereby lowering device on-resistance; rounded bottom corners alleviate local electric field concentration and enhance device breakdown voltage. Due to the high chemical stability of SiC and severe sidewall damage induced by energetic ion bombardment, conventional Si etching processes are incompatible with SiC fabrication. Therefore, a customized high-density anisotropic dry etching process with efficient sidewall protection is indispensable.

In this work, a mixed gas system consisting of SF_6, O_2, Cl_2, HBr and SiF_4 was adopted for precision SiC etching. Fluorine-containing gases provide dominant reactive radicals for chemical etching; chlorine-based gases improve etching anisotropy; O_2 eliminates polymerized byproducts; SiF_4 and HBr promote the formation of protective passivation films on both SiO_2 hard masks and SiC trench sidewalls, which suppress surface roughness and enhance SiC/SiO_2 etching selectivity. Optimized gas ratios and process parameters achieve a favorable balance between high etching efficiency and reliable sidewall protection.

Device via structures are categorized into shallow front-side vias with controllable inclination angles and high-aspect-ratio deep back-side vias. ZM shallow trenches act as physical alignment marks to resolve lithography alignment errors caused by the optical transparency of SiC substrates. Terminal edge structures form gradient mesa profiles to homogenize the surface electric field distribution and prevent premature

edge breakdown of devices.

The SJ structure is the core research focus of this work. By embedding alternating P-type and N-type doped vertical pillars within the drift layer, the structure achieves precise charge balance under reverse bias conditions. This transforms the conventional triangular electric field distribution into a uniform rectangular distribution, significantly improving device breakdown voltage. Meanwhile, heavily doped N-type pillars effectively reduce on-state conduction loss compared with traditional planar structures under identical voltage ratings.

Nevertheless, high-precision fabrication of SiC SJ trenches faces multiple technical challenges:

(1) Deep trenches (depth > 7 μm) and high aspect ratios (> 7:1) induce prominent ARDE effects;
(2) High etching selectivity is required to preserve complete patterned mask structures;
(3) Vertically aligned, ultra-smooth sidewalls, and rounded bottom profiles are mandatory for qualified devices;
(4) Consistent full-wafer uniformity and long-term process stability must be guaranteed for mass production.

To address these challenges, this work optimizes equipment configuration, gas component ratios, chamber temperature, operating pressure, and bias power. Additionally, pulsed plasma modulation and an improved Bosch etching process are implemented to suppress ARDE and refine trench morphology.

Table 1 summarizes the optimized SiC etching rates under various mixed gas atmospheres, providing reliable parametric references for process replication and tuning. The gas mixture of SF_6, O_2, Ar, and He was defined as the baseline etching recipe (Condition 1). With optimized source power, bias power, chamber pressure, and substrate temperature, a maximum SiC etching rate of approximately 2 μm/min was achieved.

Table 1. Optimized SiC etch rate range by different feed gas species.

Condition item	Feed gas species to etch SiC	SiC etch rate
1 (baseline)	$SF_6 + O_2 + Ar + He$	0.5–2.0 μm/min
2	$SF_6 + O_2 + HBr + Ar + He$	0.3–1.6 μm/min
3	$SF_6 + O_2 + SiF_4 + Ar + He$	0.2–2.1 μm/min
4	$SF_6 + O_2 + Cl_2 + Ar + He$	0.3–1.8 μm/min
5	$SF_6 + O_2 + BCl_3 + Ar + He$	0.2–1.5 μm/min
6	$Cl_2 + HBr + Ar + He$	0.1–0.5 μm/min
7	$Cl_2 + HBr + N_2 + O_2$	0.01–0.2 μm/min

When HBr (Condition 2), Cl_2 (Condition 4), or BCl_3 (Condition 5) were individually introduced into the baseline gas system, the total gas flow rate was kept constant by reducing SF_6 dosage. All three modified gas atmospheres reduced the SiC etching rate. The incorporation of an appropriate amount of SiF_4 (Condition 3) improved SiC etching efficiency, whereas excessive SiF_4 addition significantly inhibited etching progression. Both SiF_4 and HBr act as polymer precursors, facilitating

sidewall passivation and enhancing SiC/SiO_2 etching selectivity.

The combined introduction of Cl_2 and HBr (Conditions 6 and 7, without SF_6 supplementation) remarkably reduced the SiC etching rate. In particular, the synergistic reaction of Cl_2, HBr, N_2 and O_2 (Condition 7) decreased the SiC etching rate to below 0.1 μm/min.

Figure 2 presents the morphological evolution of SiC trenches before and after etching. Owing to its superior etching resistance and high patterning selectivity, SiO_2 is widely adopted as a hard mask for SiC etching, with much higher selectivity than photoresist and polysilicon masks. Prior to SiC etching, patterned SiO_2 hard masks were fabricated using a BX Honghu Coral200D dielectric etcher. Optimized etching parameters controlled the SiO_2 mask sidewall angle above 88°, laying a foundation for vertical SiC trench patterning. The initial SiO_2 mask thickness was 2.06 μm, with a final thickness of 1.87 μm after SiC etching, corresponding to a mask consumption of 0.19 μm. The maximum SiC etching depth reached 2.26 μm, achieving a SiC/SiO_2 etching selectivity exceeding 10:1. Equipped with OES real-time monitoring, the process controlled substrate recess during SiO_2 mask etching below 50 nm, ensuring excellent process repeatability.

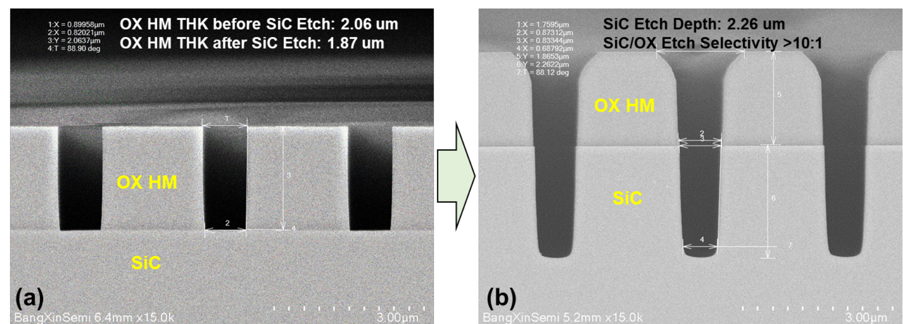

Figure 2. SiC trench structure before and after etching: **(a)** Before SiC etching; **(b)** After SiC etching.

Subsequent pattern transfer and SiC etching were implemented using the BX Honghu Ivory200SCE ICP etcher. The equipment delivers strong anisotropic etching capability to break robust Si–C bonds and realize high-fidelity vertical pattern transfer. The verticality of fabricated SiC trenches is directly determined by the sidewall quality of pre-patterned SiO_2 hard masks. Through systematic hardware optimization and parametric tuning, the SiC/SiO_2 etching selectivity was stably maintained above 10:1, enabling the fabrication of deeper trenches with limited mask thickness, which is critical for the mass production of high-aspect-ratio SJ devices.

Figure 3 displays optimized SiC trench structures with aspect ratios ranging from 3:1 to 15:1. All samples adopted SiO_2 hard masks, and diverse aspect ratios were achieved by tuning gas ratios, chamber pressure, and RF power under consistent equipment configuration, with a maximum trench depth exceeding 21 μm. For trenches with aspect ratios of 3:1, 10:1, and 15:1, the corresponding SiO_2 mask consumption was 0.2 μm, 0.75 μm and 1.5 μm, yielding etching selectivities of 11.5, 10.3, and 14.1, respectively.

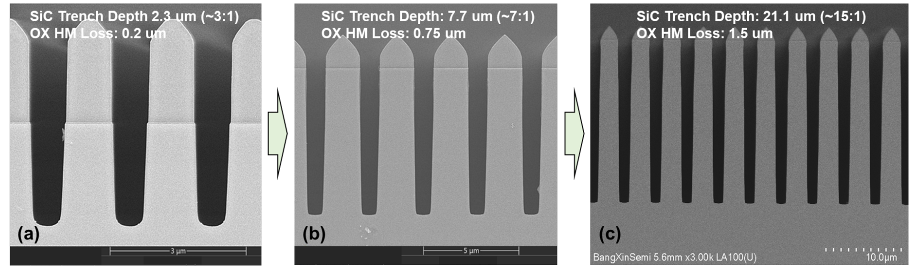

Figure 3. SiC trench structures with different AR: **(a)** 3:1; **(b)** 10:1; **(c)** 15:1.

For deep trench etching exceeding 21 μm, the SiO_2 hard mask thickness was increased to over 5 μm. Thickened hard masks withstand prolonged plasma etching and ion bombardment, preserve trench top CD and corner morphology, and maintain sidewall angles above 88° throughout deep etching processes. This approach effectively eliminates tapered profile defects caused by excessive mask erosion. The successful fabrication of high-aspect-ratio deep trenches establishes a solid process foundation for ultra-high-voltage SiC SJ device manufacturing.

Table 2 summarizes the influences of key process parameters on SiC trench profiles based on full-scale 8-inch wafer tests, revealing the tuning rules of center-edge profile deviation, top-bottom CD offset, and dense-isolated (dense-ISO) micro-trench effects. The incorporation of SiF_4, elevated chamber pressure, and enhanced RF bias power collectively improve SiC etching rates. As a functional precursor, SiF_4 promotes the formation of fluorocarbon passivation films to protect trench sidewalls and optimize ISO pattern inclination angles, while providing abundant fluorine radicals to accelerate chemical etching reactions.

Table 2. Effects of etching process parameters on SiC trench profile (8-inch wafer testing).

Condition	Side wall angle	SiC ER	C/E loading (dense)	Micro trench (dense & ISO pattern)	CD bias (BCD-TCD)	SiC/OX Sel.	Line-end striation	Sidewall bowing
SiF_4+	Dense Keep, ISO↓	C↑, E Keep	↑	Dense Keep, ISO Worse	C & E↑	↑	Better	C & E better
Pressure+	Dense Keep, ISO↓	C & E↑	Keep	Dense/ISO Keep	C & E↑	↑	/	C better
Bias+	Dense↑, ISO Keep	C Keep, E↑	↓	Dense & ISO Better	Keep	↓	/	E worse
Ar & He+	Dense Keep, ISO↑	C & E↓	↓	Dense Better, ISO Keep	↓	↓	/	/
O_2+	Dense ↓, ISO C↓	C & E↓	↑	Dense Keep, ISO Worse	C↑E↓	↑	Better	/

Micro-trenching at trench bottom corners originates from three primary mechanisms: scattered ion bombardment-induced local etching enhancement, uneven polymer passivation film distribution at trench bottoms, and electrostatic aggregation of charged byproducts that attracts incident ions toward corner regions. These adverse effects can be effectively mitigated via precise process tuning. For high-aspect-ratio deep trench fabrication, chamber pressure, gas composition, and bias power are the dominant control parameters. Polymerizable gases (e.g., SiF_4) form uniform thin passivation layers on trench sidewalls, which suppress lateral etching, reduce mask consumption, improve SiC/SiO_2 selectivity, and stabilize dimensional consistency. Moderate chamber pressure balances the formation and desorption of passivation

polymers to prevent profile distortion. A dedicated post-etch bottom rounding process was integrated to optimize corner morphology, relieve electric field concentration, and improve device breakdown performance and long-term reliability.

The morphological evolution of SiC trenches is governed by the competitive coupling effect between chemical radical etching and physical ion bombardment. Increased bias power enhances etching anisotropy but may elevate sidewall roughness; appropriate chamber pressure homogenizes radical distribution and alleviates the ARDE effect. Polymer passivation precisely balances vertical etching progression and lateral sidewall protection.

Figure 4 presents tilted SEM images of the SiC SJ trench bottom morphology. Obvious striation-shaped roughness was observed on SiC trench sidewalls, with identical morphological defects on the upper SiO_2 hard mask sidewalls, verifying severe sidewall roughness transfer from SiO_2 masks to SiC layers during etching.

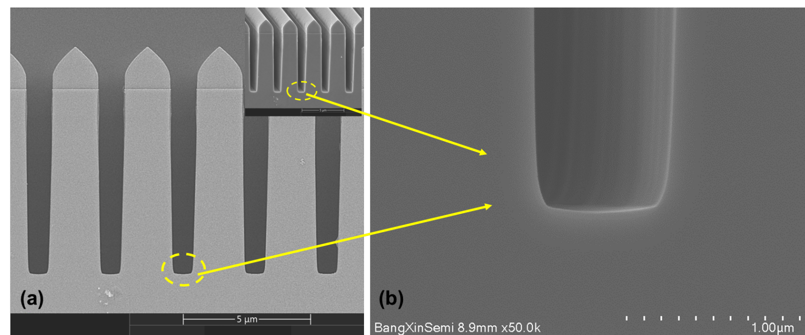

Figure 4. Tilted-view SEM image of the bottom morphology of a SiC SJ structure: **(a)** Overall view; **(b)** Magnified view of sidewall striations.

Accordingly, optimizing SiO_2 hard mask sidewall quality and suppressing roughness transfer are critical for high-precision SiC trench fabrication, as preliminarily verified in our previous work [31]. The sidewall roughness of SiO_2 masks can be significantly reduced by refining the lithography and coating process of initial photoresist layers and implementing post-etch smoothing treatment on patterned SiO_2 masks. Since SiC etching requires intense ion bombardment to break high-strength Si–C bonds, residual microscopic defects on SiO_2 mask sidewalls are easily transferred and amplified on SiC trench surfaces. Therefore, precise parameter calibration, rational gas selection, and accurate pressure regulation are essential for high-quality deep SJ trench etching. As validated experimentally, polymer-forming gases effectively protect both SiO_2 hard masks and SiC trench sidewalls. Despite effective sidewall optimization, bottom corner rounding still requires further refinement, which is realized via an additional post-main-etch corner smoothing process in this work.

Figure 5 further elucidates the sidewall roughness transfer mechanism from oxide hard masks to SiC trenches. Given the high Si–O bond energy (460 kJ/mol), SiO_2 mask patterning also requires intensive vertical ion bombardment, which replicates micro-striation defects originating from photoresist sidewalls onto oxide mask surfaces. Two targeted optimization strategies were proposed to address this issue. First, at the mask preparation stage, the photoresist spin-coating and lithography processes were optimized, and post-etch smoothing treatment was performed on SiO_2 masks to

reduce initial sidewall roughness. Second, after SiC main etching, a low-rate isotropic smoothing process was implemented. By elevating chamber pressure, optimizing substrate temperature, and reducing reactive radical concentration, micro-defects on SiC trench sidewalls were repaired to minimize surface roughness.

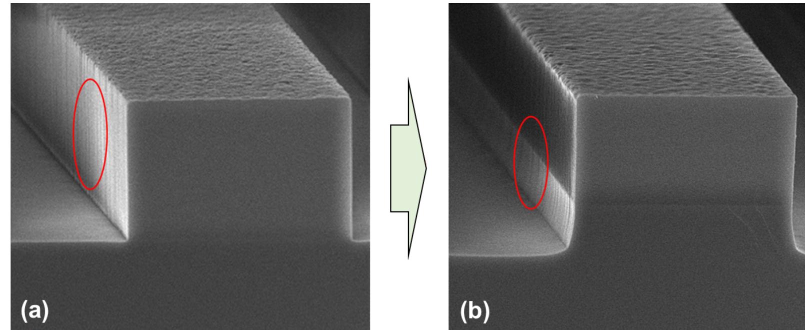

Figure 5. Sidewall roughness (striation) transfer from oxide hard mask to SiC trench: **(a)** Striations on oxide hard mask; **(b)** Transferred striations on SiC sidewall.

Previous experimental results [31] confirm that the above dual optimization strategies effectively suppress roughness transfer and significantly improve SiC trench sidewall quality. A specialized BX Honghu Garnet200I etching system can also be adopted for SiC sidewall surface treatment via chemical dry etching mechanisms, which completely eliminates physical ion bombardment damage.

Table 3 summarizes the full-wafer etching uniformity of 8-inch SiC SJ structures. All tested samples feature trench depths exceeding 7 μm and aspect ratios above 7:1. Full-wafer uniformity was quantitatively evaluated by measuring trench CD, etching depth, and sidewall angle at five discrete positions across 8-inch wafers, followed by standard deviation and variation range calculation.

Table 3. Full-wafer (8 inch) etching uniformity of SiC SJ structure.

Super-junction structure	**Structure**	**Center**	**Edge top**	**Edge bottom**	**Edge right**	**Edge left**	**U%**
Items for Full-Wafer Uniformity	Figure						U% = (Max−Min)/2Avg.
	TCD (μm)	1.03	1.03	1.03	1.03	1.05	0.97%
	BCD (μm)	0.83	0.85	0.83	0.83	0.83	1.20%
	Depth (μm)	7.18	7.16	7.24	7.24	7.26	0.69%
	Angle (>88°)	88.8°	88.5°	88.9°	88.8°	88.6°	>88°

After systematic process optimization, the full-wafer CD variation was controlled below 2%, the etching depth uniformity was superior to 1%, and the sidewall angles at both wafer center and edge positions remained above 88%. Cross-position structural measurement confirms consistent top-to-bottom profile uniformity of SiC SJ trenches across the entire wafer, achieving excellent large-area fabrication uniformity.

The improved full-wafer uniformity benefits from multi-dimensional equipment collaborative optimization:

(1) A dual-zone coil system independently adjusts RF power distribution to

homogenize plasma density across wafer center and edge regions;

(2) A zoned gas injection system optimizes surface gas concentration distribution to improve radial etching uniformity;

(3) A dual-zone helium backside cooling system precisely regulates wafer temperature distribution, stabilizing etching selectivity and sidewall angle consistency;

(4) Independent tuning gas injection further compensates for performance deviations between the wafer center and edge.

The synergistic effect of the above optimization methods realizes high-precision full-wafer etching, fully meeting large-scale industrial manufacturing requirements.

Figure 6 presents the long-term stability test results of the 8-inch Ivory200SCE SiC etching system. Standard monitor wafers were processed under identical baseline conditions for 10 consecutive months to evaluate equipment and process stability. The results reveal excellent stability: etch rate variation was within 3%, and full-wafer uniformity remained below 2% over the monitoring period. The excellent performance stems from stable plasma chemistry, precise gas regulation, robust chamber-wall quality, uniform wafer cooling, and a strict wafer-to-wafer cleaning procedure that suppress plasma drift and particle contamination and maintain a stable chamber environment. Such long-term repeatability minimizes process-induced device fluctuations, improves yield, and reduces costs, confirming the industrial mass-production feasibility of the proposed SiC SJ trench etching process.

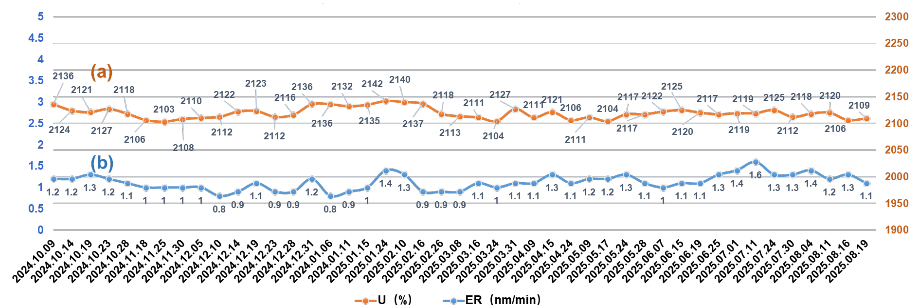

Figure 6. Long-term stability of the SiC etching tool.

Note: Line (a) etch rate variation over 10 months; Line (b) uniformity variation over 10 months.

4. Conclusion

This work systematically investigates the precision etching and patterning technologies of ultra-high-voltage SiC SJ power devices. Comprehensive mechanism analysis and parametric optimization were performed, focusing on high-aspect-ratio deep trench fabrication, sidewall roughness suppression, full-wafer uniformity improvement, and long-term process stability. Through optimized gas combinations, process parameter calibration, and equipment configuration tuning, SiC trenches with aspect ratios ranging from 3:1 to 15:1 and maximum depths over 21 μm were successfully fabricated, with stable SiC/SiO_2 etching selectivity above 10:1. This resolves the core technical challenges restricting high-quality SiC SJ trench manufacturing.

Furthermore, this study clarifies the physical mechanism of sidewall roughness transfer from SiO_2 hard masks to SiC trenches. Targeted optimization strategies, including refined mask fabrication, polymer-based sidewall passivation, and post-etch smoothing treatment, were proposed to significantly improve trench sidewall surface quality. Multi-dimensional equipment tuning synergistically enhances 8-inch full-wafer fabrication uniformity, achieving CD variation below 2%, etching depth uniformity superior to 1%, and consistent sidewall angles above 88%, which satisfies large-diameter wafer industrial manufacturing standards.

Ten months of continuous mass-production monitoring verify that the developed process achieves etching rate fluctuation within 3% and uniformity variation below 2%, demonstrating excellent repeatability and manufacturability. This work realizes key technical breakthroughs in high-aspect-ratio SiC SJ trench etching, breaks the core process bottlenecks for ultra-high-voltage high-efficiency SiC power device industrialization, provides a reliable fabrication solution for high-performance third-generation semiconductor devices, and promotes the commercial application and technological development of SiC power electronics.

Author contributions: Conceptualization was performed by SW, JL (Jie Liang) and ZW; The SiC etching process was conducted, and the data were summarized by SW, MZ, JL (Jian Li), JZ, QW, DH and HQ; The original draft was prepared by SW, and review and editing were carried out by SW and ZW; Etching tool resources were provided by ZG, LT and JL (Jie Liang). All authors have read and agreed to the published version of the manuscript.

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Informed consent statement: Not applicable.

Data availability statement: This work was carried out at multiple R&D facilities of Shanghai BangXin Semi Technology Co., Ltd.; the experimental data were acquired using the following equipment: ICP etcher (Ivory150/200SCE), scanning electron microscope (Hitachi SU8600), and film thickness tester (NANO metrics).

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Abbreviations

SiC	Silicon Carbide
SJ	Super-Junction
CD	Critical Dimension
ARDE	aspect Ratio Dependent Etching
RF	Radio Frequency
ICP	Inductively Coupled Plasma
CMP	Chemical Mechanical Polishing
PECVD	Plasma-Enhanced Chemical Vapor Deposition
ESC	Electrostatic Chuck
SEM	Scanning Electron Microscopy
TEM	Transmission Electron Microscopy
AFM	Transmission Electron Microscopy
OES	Optical Emission Spectroscopy

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