Energy Storage and Conversion 2024, 2(1), 426.
https://doi.org/10.59400/esc.v2i1.426

Article

Nonlinear controller for SEPIC with single variable to tune

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CITATION

El Haj Y, Sood V, Sheir A, Milman R. Nonlinear controller for SEPIC with single variable to tune. Energy Storage and Conversion. 2024; 2(1): 426.
https://doi.org/10.59400/esc.v2i1.426

ARTICLE INFO

Received: 22 December 2023
Accepted: 22 January 2024
Available online: 29 January 2024

Abstract: This work proposes a systematic approach to designing a novel integral sliding mode controller (ISMC) for a single-ended primary-inductor converter (SEPIC) with only one tunable parameter where the upper and lower bounds are derived. The designed surface results in minimal chattering behaviour at the output voltage as well as at the duty cycle and allows for operating the SEPIC at a fixed switching frequency. The proposed controller can withstand up to a 70% variation in the input voltage and 100% variation on the load side, in addition to superior performance for a cold start. The proposed controller and the corresponding mathematical formulation were simulated in a Simulink environment and experimentally tested via a scaled prototype. The proposed controller performance is also compared to Type II and integral Linear-Quadratic Regulators (LQR).

Keywords: SEPIC; ISMC; systematic design; nonlinear controller

1. Introduction

Different types of controllers are designed to achieve one or more objectives based on the target application [1]. For example, in low-power electronic circuits, controlling the converter's output power is the main design objective. This can be extended to different applications, such as LED drives in lighting applications, where the lights can be dimmed by adjusting the converter's output voltage. A battery charging application is another application where the controller is designed to serve objectives such as output current and voltage control. This is expandable to grid-connected renewable energy sources and motor drive applications as well [1–3].

Within the field of power converters, the performance of the designed controller is evaluated and measured based on four metrics: 1) steady-state gain and regulation; 2) dynamic response to load and input disturbances; 3) compliance to electromagnetic interference (EMI) standards and/or total harmonic distortion (THD) regulations; and 4) contribution to converter protection schemes such as overcurrent protection and inrush current limiting. In addition, many controllers are designed not only to satisfy the converter's input-output regulation and performance metrics but also to improve its performance under intrinsic uncertainties, such as components' parasitic capacitance and inductance variations due to soft/ hard saturations [1,4–6]. Therefore, diverse types of control schemes are implemented to achieve as many design objectives as possible. The simplest approach is direct output current control, where a sense of the output voltage provides the correction signal to the controller, which adjusts the converter's duty cycle to maintain the output voltage at or near its reference setting. Such controllers lack the ability to contribute to the converter's protection scheme in terms of short-circuit protection. Other control schemes, such as peak current control and average current control, indirectly control the converter's output

voltage by regulating the internal states, such as the inductor current. The advantage of such schemes is that they satisfy the majority of the controller design objectives while contributing to other aspects of its performance evaluation, such as fast transients and one-cycle short circuit protection [7].

Furthermore, from a controller's law point of view, they can be classified as either linear or nonlinear controllers. Examples of linear controllers are proportional-integral (PI) controllers, type II-III compensators, LQR controllers, and state feedback controllers [4,8]. On the other hand, hysteresis controllers, adaptive controllers, and sliding mode controllers are examples of nonlinear controllers in power electronics. While linear controllers are designed based on the converter's linearized model, they suffer from the severe disadvantage of being able to maintain their performance within narrow regions around the linearized point. On the contrary, nonlinear controllers offer superior performance in terms of satisfying their design objectives and performance metrics over a wider range of load disturbances, input disturbances, parameter uncertainties, and noise [9–14].

Among nonlinear controllers, the sliding mode controller (SMC) has the most attention in both discrete and continuous forms [15]. SMC has a variable structure in its dynamics, ensures disturbance and uncertainty rejection, and performs robust tracking tasks. For instance, in the study of Hamed et al. [15], a modified SMC is designed for a buck converter, and its performance is compared against different types of linear and nonlinear controllers. The study shows that the proposed modified SMC has superior characteristics and fast dynamics. Nonetheless, it is reported that the proposed modified SMC was not able to overcome the chattering phenomenon associated with SMC controllers in general. It also only includes the study of a well-behaved buck converter without explaining how such a controller can be extended to converters with right half-plane zeros or higher-order converters such as SEPIC converters.

An improved SMC for output voltage control in a boost converter is developed in the study of Chincholkar et al. [16]. The proposed controller is applied to a boost converter and compared against PI controllers. Although the research incorporates an integral term, which is a function of the normalized output voltage error, no details were provided on how to solve the chattering issue in the converter's output control signal (duty cycle) or on how to extend this controller to higher-order converters [10,17].

Another approach is introduced in the study of González et al. [18] to overcome the chattering in SMC. In the work, a PI controller is used to form an outer control loop to form a double control loop with the SMC in discontinuous conduction mode (DCM) buck-boost converter. This technique was able to improve the converter's dynamic and steady-state performance. However, it is based on a hysteresis-based SMC, which requires an adaptive feed-forward controller to reduce switching frequency variation. Such frequency restriction is instrumental in reducing EMI noise and input filter design complexity.

A solution to the chattering phenomenon in SMC in power electronics is introduced in the study of Pamdey et al. [19], Ghosh et al. [20], and Das et al. [21]. An integral SMC is developed, which solves the chattering issue in the control signal. This is done by incorporating an integral term to average the output control signal, which

eliminates the chattering and confines the switching frequency to a single frequency. However, the introduced work only covers the design procedure of second-order converters such as buck and boost converters. It also does not cover the converter tuning process that balances the reduction of the chattering of the control signal with the desired dynamic performance.

Furthermore, optimization techniques and artificial intelligence-based SMC design are also introduced [3,12–14,22–25]. It is undeniably beneficial to integrate such techniques with advanced nonlinear controllers such as SMC. It restricts the extension of such algorithms to lower-power and high-density high-power applications where more powerful digital controllers are not available due to size or cost constraints.

In this work, an integral-based SMC is proposed with a systematic approach to design a nonlinear SMC that has not been presented earlier and outlined for high-order converters such as a SEPIC. The main advantage of the proposed controller is that it needs a single value to be tuned over a defined interval with calculated upper and lower bounds. Further, the proposed sliding surface is simple with respect to other proposed sliding surfaces mentioned in the literature. It should be highlighted that the proposed SMC did not compromise the robustness and stability of the system because it was derived based on the dynamics of the converter, where the role of the surface elements was explained and justified. The nonlinearity aspect of the derived SMC rejects varying input voltage disturbances over a wide range. The proposed work is first theoretically proven and then validated by simulation and experimental work. To establish a benchmark with a linear controller, traditional Type-II as well as integral LQR compensators are designed, simulated, and compared with the proposed controller. Furthermore, to complete the comparison analysis between the linear controller and the proposed ISMC, the Type-II compensator will be compared experimentally to the proposed controller. The comparison includes three test categories: cold start, input voltage variation, and load disturbance tests.

The rest of the paper is organized as follows: Section 2 discusses the SEPIC and sliding mode controllers. Section 3 provides the detailed design and modeling of the SEPIC converter. Section 4 deals with the linear and nonlinear controller overview and design for the SEPIC converter. Section 5 provides a derivation of the proposed controller and a step-by-step design guide. Section 6 gives the stability analysis of the proposed controller using the Lyapunov methodology. Section 7 provides the simulation and experimental results of three types of compensators: the Type II compensator, the integral LQR, and the proposed controller. Finally, Section 8 gives concluding remarks on the work presented.

2. SEPIC and sliding mode

The single-ended primary inductor converter (SEPIC) is a fourth-order DC-DC converter. Its large-signal model is highly nonlinear and demonstrates bi-linearity with respect to the control input. Linearized controllers are only valid in a small neighborhood around the equilibrium point, resulting in systems that are vulnerable to instability when faced with any disturbance away from the linearized region. To tackle this issue, a nonlinear controller that provides stable performance over the entire

nonlinear model becomes essential, especially in applications where cost, stability, and performance are critical criteria to maintain, such as integrating renewable energy into the grid and electric vehicles.

Among the nonlinear controller alternatives, the sliding mode controller has an edge with respect to others such as backstepping and feedback linearization. This is because sliding mode control has a variable structure controller that ensures disturbance and uncertainty rejection while performing robust tracking of the desired trajectory. Since DC-DC converters are based on switching mechanisms where the structure varies momentarily based on the switching cycle, a sliding mode controller appropriately complements the application's behaviour.

Different designs for sliding mode control of the SEPIC converter have been addressed in the literature. The work presented in the study of Gireesh et al. [26] uses a pulse width modulated (PWM)-based integral sliding mode control (ISMC) strategy for controlling the output voltage of a SEPIC converter. The work designed an ISMC to regulate the output voltage. The input voltage was varied from 3 to 7 V, while the output was kept at 5 V. The load variation itself was not tested. The output plot had a minor steady-state tracking error. The sliding surface was designed as an error function using the input current, output voltage, and the integral of both voltage and current errors. That sliding surface requires a definition of a reference current for the input inductor. The system is driven based on a PWM signal that is generated based on the equivalent control principle with no switching signal in the control law. On the contrary, the study of Salazar-Duque et al. [27] simplified the sliding surface to be a function of the inductor's current. The reference currents were assigned as the steady-state values of the currents. The controller was tested in two cases. In case I, the input voltage was 24 V, while the reference was changing from 8 to 30 V. In case II, the input voltage was 19 V, and the reference was varied again from 8 to 30 V. The control law was dependent on switching signals with no indication of how it was performed (hysteresis or PWM approach). The system was not tested for variation in the input voltage during the operation or for load variation.

As discussed above, SEPIC converters have the inherent tendency to experience chaotic behaviour as shown in the study of Kavitha et al. [28]. To overcome the instability of the system, an SMC controller was proposed that used a sliding surface composed of the inductor current signal subtracted from a reference value. The desired duty cycle was generated using a hysteresis controller. The system did not investigate the impact of varying either the input, the voltage, or the load on the output behaviour.

Given the fact that robustness is one of the most vital criteria to evaluate the performance of a converter, the researchers in the field proposed another design to ensure a robust response of the SEPIC converter, as demonstrated in the studies of Ablay et al. [29], Li et al. [30], Komurcigil et al. [31], and Jaafar et al. [32]. In the study of Ablay et al. [29], the paper proposed an integral sliding mode controller (ISMC) by defining a surface composed of the negative of the input inductor current and the integral of the error of the output voltage. The surface is simple and proves its ability to track the reference value. The input voltage was 15 V, while the reference voltage varied from 8–25 V. The work proposed a laboratory setup for the controller made of analog components. The control signal was switched using an on/off-based (hysteresis) technique depending on the sign of the sliding surface, which results in a

variable-frequency pulse width modulation (PWM) signal. The system was not tested against variations in either the input voltage or the load impedance. Furthermore, this work used only a simulation study, and experimental results were not presented. Also, the work did not justify how the surface was constructed or the role of the surface elements in system performance and stability. Additionally, from a mathematical perspective, the utilization of the negative current will oppose the surface trajectory, which will result in accumulating more error in the integral function, which may eventually result in slow responses. Alternatively, the system may result in an undesired transient oscillation to make the system reach faster to the desired equilibrium points, given that the scaling factors of the error functions are pre-selected and strong enough to ride the system towards the desired trajectories. From the Lyapunov stability perspective, this type of surface does not ensure negative definite functions under the analysis of a typical Lyapunov candidate function for an SMC; hence, the stability should be studied further.

A universal design has been illustrated in the study of Li et al. [30], where the work proposed a double integral sliding mode controller (DISMC) to control a SEPIC converter. The proposed design was implemented on FPGA and DSP boards operating at 500 kHz and 20 kHz, respectively. The sliding surface was composed of errors in the input inductor current, errors in the output voltage, single and double integrals of the current, and voltage error summation. The controller was operated using a PWM technique. The algorithm was tested by reducing the load from 40 to 20 ohms.

Designing a robust system with a simple design structure is highly recommended. To adhere to this requirement, a simple sliding surface composed of the error in the input inductor current was proposed in the study of Komurcugil et al. [31]. The reference current was generated by a PI controller, which takes its input by measuring the output voltage. The control signal was generated using a hysteresis controller. The controller was tested against input variations where the input was varied from 30–60 V while the output was maintained at a fixed level of 48 V. The load was varied from 50–100 ohms and vice versa. The effect of combining the two variations (load and input voltage) was not shown.

To define the structure of the sliding surface, the study of Jaafar et al. [32] proved the instability of sliding surfaces composed only of any combination of output error voltage, including the error itself, its integral, and its derivative. The work proved the requirement of including at least the error in the input inductor current in addition to the previously defined surfaces. The control signal was derived based on the equivalent control that is free from the switching function. Nevertheless, neither a variation in the input voltage nor in the load was discussed.

Based on the addressed literature, there is a gap in investigating the impact of integrating fast dynamic and variable power resources where the input voltage declines, such as a supercapacitor, as an input to the SEPIC converter. Designing a stable SEPIC converter in buck and boost operation that can withstand major input voltage variation as well as output load variation will allow a resilient and wider range of integration of hybrid energy sources in different fields, such as microgrid-connected fields and electric vehicles.

The prime challenge in this work is to integrate input power sources that drop significantly (primarily to mimic supercapacitor behaviour) with the SEPIC converter

because a typical linear controller fails to achieve the desired response and may impact system stability. Furthermore, the design of a SEPIC controller is a challenging task from both linear and nonlinear controller perspectives. This is because linear controllers for SEPIC converters result in a system with low bandwidth, while the nonlinear controller design method has not been addressed in the literature in a systematic way, unlike linear controllers. In fact, the controllers discussed in the literature suffered from different disadvantages and limitations, as discussed earlier in this chapter. Further details explaining what makes designing a SEPIC controller a challenging task will be covered in the next section.

3. Design and modeling of SEPIC converter

3.1. Mathematical modeling of SEPIC converter

In the DC/DC converter family, the standard SEPIC converter (**Figure 1**) can both buck and boost the DC input voltage. The basic topology of a SEPIC converter is composed of two inductors, two capacitors, a switch, and a diode. SEPIC is classified as a fourth-order converter based on the number of energy storage devices.

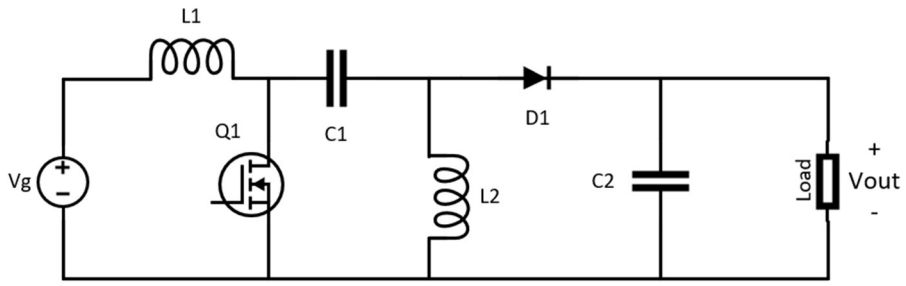


Figure 1. Standard SEPIC circuit.

By controlling the duty cycle (D) of the switch, the SEPIC converter will exhibit a switching mechanism that will result in stepping up or down the input voltage. The input-output relationship with respect to the duty cycle D is given in Equation (1):

$$\frac{v_{out}}{v_g} = \frac{D}{1-D} \tag{1}$$

where D is the duty cycle of the switch.

Specifically, the output of the SEPIC as a function of the duty cycle is summarized as follows:

$$\text{If } D = \begin{cases} < 0.5 & v_{out} < v_{in} \rightarrow \text{Buck mode} \\ = 0.5 & \text{then } v_{out} = v_{in} \\ > 0.5 & v_{out} > v_{in} \rightarrow \text{Boost mode} \end{cases} \tag{2}$$

Deriving the averaged state-space model of the DC-DC power converter is done in two steps. The first step in deriving the averaged model of the SEPIC is to address the converter dynamics while the switch is in the "on" and the "off" states. In the second step, the two sets of differential equations corresponding to the on and off states are averaged over one switching cycle.

Thus, when the switch is in the on position, the SEPIC converter is given in **Figure 2**.

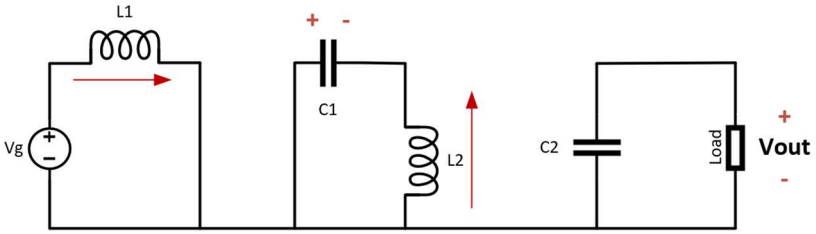


Figure 2. SEPIC converter when the switch is on.

The system's differential equations are defined as:

$$\begin{aligned} \boldsymbol{v_{L1} = L_1 \frac{di_{L1}}{dt} = v_g(t) - r_{L1} i_{L1}} \\ \boldsymbol{v_{L2} = L_2 \frac{di_{L2}}{dt} = v_{c1}(t) - r_{L2} i_{L2}} \\ \boldsymbol{i_{C1} = C_1 \frac{dv_{C1}}{dt} = -i_{L2}(t)} \\ i_{C2} = C_2 \frac{dv_{C2}}{dt} = -\frac{v_{c2}(t)}{R} \end{aligned} \tag{3}$$

When the switch is turned off, the converter model is shown in **Figure 3**.

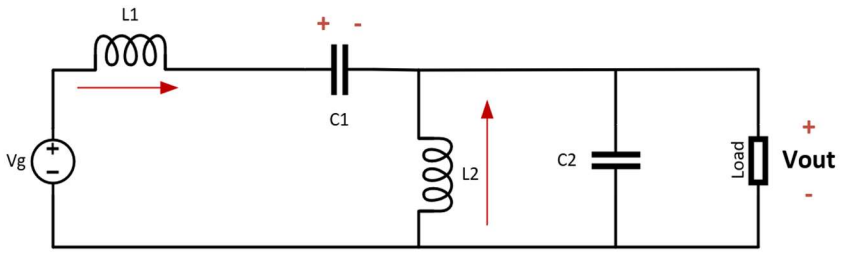


Figure 3. SEPIC converter when the switch is off.

Analyzing the system, the following differential equations are derived:

$$\begin{aligned} \boldsymbol{v_{L1} = L_1 \frac{di_{L1}}{dt} = v_g(t) - v_{C1}(t) - v_{C2}(t) - r_{L1} i_{L1}} \\ \boldsymbol{v_{L2} = L_2 \frac{di_{L2}}{dt} = -v_{c2}(t) - r_{L2} i_{L2}} \\ \boldsymbol{i_{C1} = C_1 \frac{dv_1}{dt} = i_{L1}(t)} \\ i_{C2} = C_2 \frac{dv_2}{dt} = i_{L1}(t) + i_{L2}(t) - \frac{v_{c2}(t)}{R} \end{aligned} \tag{4}$$

Using Equations (3) and (4) in state space representation, the averaged model of the SEPIC converter can be derived using the relationship defined in Equation (5):

$$\begin{aligned} \boldsymbol{A_{avg} = A_1 u(t) + A_2 \big(1 - u(t)\big)}, \\ B_{avg} = B_1 u(t) + B_2 \big(1 - u(t)\big), \end{aligned} \tag{5}$$

where $u(t)$ is the system input, A_1 and B_1 are the system input matrices respectively when the switch is on and A_2 and B_2 are the system and the input matrices respectively when the switch is off.

The average state-space representation for the SEPIC converter is obtained and expressed in Equation (6):

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \\ \dot{x_3} \\ \dot{x_4} \end{bmatrix} = \begin{bmatrix} -\frac{r_{L1}}{L_1} & 0 & -\frac{1-u}{L_1} & -\frac{1-u}{L_1} \\ 0 & -\frac{r_{L2}}{L_2} & \frac{u}{L_2} & -\frac{1-u}{L_2} \\ \frac{1-u}{C_1} & -\frac{u}{C_1} & 0 & 0 \\ \frac{1-u}{C_2} & \frac{1-u}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + \begin{bmatrix} \frac{V_g}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}, \tag{6}$$

where $x_1 = i_{L1}$, $x_2 = i_{L2}$, $x_3 = v_{C1}$, $x_4 = v_{C2}$, and v_g =input voltage.

As demonstrated in Equation (6), this model addresses the equivalent series resistance (ESR) of the inductors while the capacitors' ESR has been suppressed because the inductor ESR is dominant with respect to capacitor parasitic.

From a linear controller perspective, the SEPIC model in Equation (6) is still in bilinear form and cannot be used to design a linear controller. Therefore, this form must be linearized, where the linearized model will define a relationship between the system controller input and the state variables. Hence, by perturbing the state variables, considering small signal approximations, and then linearizing the derived terms, the small signal model in state-space representation is obtained as below.

$$\boldsymbol{A} = \begin{bmatrix} \boldsymbol{0} & \boldsymbol{0} & -\frac{\boldsymbol{1-D_u}}{\boldsymbol{L_1}} & -\frac{\boldsymbol{1-D_u}}{\boldsymbol{L_1}} \\ \boldsymbol{0} & \boldsymbol{0} & \frac{\boldsymbol{Du}}{\boldsymbol{L_2}} & -\frac{\boldsymbol{1-D_u}}{\boldsymbol{L_2}} \\ \frac{\boldsymbol{1-D_u}}{\boldsymbol{C_1}} & -\frac{\boldsymbol{D_u}}{\boldsymbol{C_1}} & \boldsymbol{0} & \boldsymbol{0} \\ \frac{\boldsymbol{1-D_u}}{\boldsymbol{C_2}} & \frac{\boldsymbol{1-D_u}}{\boldsymbol{C_2}} & \boldsymbol{0} & -\frac{\boldsymbol{1}}{\boldsymbol{RC_2}} \end{bmatrix},$$

$$\boldsymbol{B} = \begin{bmatrix} \frac{\boldsymbol{v_{1_{ss}} + v_{2_{ss}}}}{\boldsymbol{L_1}} \\ \frac{\boldsymbol{v_{1_{ss}} + v_{2_{ss}}}}{\boldsymbol{L_2}} \\ \frac{\boldsymbol{-i_{1_{ss}} - i_{2_{ss}}}}{\boldsymbol{C_1}} \\ \frac{\boldsymbol{-i_{1_{ss}} - i_{2_{ss}}}}{\boldsymbol{C_2}} \end{bmatrix}, \boldsymbol{C} = [\boldsymbol{0\ 0\ 0\ 1}], \boldsymbol{D} = \boldsymbol{0}, \boldsymbol{x} = \begin{bmatrix} \boldsymbol{x_1} \\ \boldsymbol{x_2} \\ \boldsymbol{x_3} \\ \boldsymbol{x_4} \end{bmatrix} \tag{7}$$

where: $i_{1_{ss}} = \frac{D_u^2}{(1-D_u)^2}\frac{v_g}{R}$, $i_{2_{ss}} = \frac{D_u}{1-D_u}\frac{v_g}{R}$, $v_{1_{ss}} = v_g$ and $v_{2_{ss}} = \frac{D_u}{1-D_u}v_g$.

The derived linear state-space model is effective in designing linear controllers that require knowledge of each state dynamic, such as state feedback and its optimized version, LQR. Other standard linear controllers (such as PID family and lead/lag compensators) require only a transfer function that describes a relationship between the control variable and the output voltage if the goal is to regulate the output voltage. In the literature, extensive work has been done to define this transfer function in the study of Basso [33], and this model is given in Equation (8).

Within the scope of this work, the discussed three models of SEPIC converter will be used to design the proposed ISMC, integral LQR, and Type-II compensator, while the system response will be simulated on the switched bilinear model using

MATLAB/Simulink package. Furthermore, the designed controllers will be verified with experimental benchwork using a SEPIC converter.

$$\frac{\boldsymbol{v_{out}}}{\boldsymbol{u}}(\boldsymbol{s}) = \boldsymbol{K_d}\frac{(-\boldsymbol{A_1 s}+\boldsymbol{1})(\boldsymbol{A_2 s^2}-\boldsymbol{A_3 s}+\boldsymbol{1})}{(\boldsymbol{A_4 s^2}+\boldsymbol{A_5 s}+\boldsymbol{1})(\boldsymbol{A_6 s^2}+\boldsymbol{A_7 s}+\boldsymbol{1})} \tag{8}$$

where: $K_d = \frac{1}{(D')^2}$ and $D' = 1 - D$, and D is the duty cycle. $A_1 = \left(\frac{L_1}{R}\right)\left(\left(\frac{D}{D'}\right)^2\right)$, $A_2 = L_2\frac{C_1}{D}$, $A_3 = \left(C_1 R\frac{L_1+L_2}{L_1}\right)\left(\left(\frac{D'}{D}\right)^2\right)$, $A_4 = \frac{1}{w_{o1}^2}$, $A_5 = \frac{1}{w_{o1}Q_1}$, $A_6 = \frac{1}{w_{o2}^2}$, $A_7 = \frac{1}{w_{o2}Q_2}$, $w_{o1} = \frac{1}{\sqrt{\left(\left(L_1\left(\left(C_2\frac{D^2}{D'^2}\right)+(C_1)\right)\right)+(L_2(C_1+C_2))\right)}}$, $Q_1 = \frac{R}{w_{o1}\left(\left(L_1\left(\frac{D^2}{D'^2}\right)\right)+L_2\right)}$, $w_{o2} = \sqrt{\left(\left(\frac{D'^2}{L_1L_2C_1C_2}\right)\left(\left(L_1\left(C_2\left(\left(\frac{D}{D'}\right)^2\right)+C_1\right)\right)+(L_2(C_1+C_2))\right)\right)}$, $Q_2 = \frac{R}{w_{o2}(L_1+L_2)\left(\frac{C_1}{C_2}\right)\left(\frac{w_{o1}}{w_{o2}}\right)^2}$.

3.2. Design of SEPIC converter

In this work, the foundation of the analysis is based on a proper design for a SEPIC converter. Typically, the circuit parameters of the SEPIC converter play a key role in the controller's bandwidth as well as its robustness. This is evident through analyzing the Bode plot of G_{vd} transfer function (i.e., the output voltage to duty cycle transfer function). Typical bode plots of G_{vd} show that SEPIC has double resonance peaks due to the existence of three right half-plane zeros. Additionally, the second resonance is much higher than the first, which impacts the system bandwidth at closed loop. Therefore, it is essential to ensure that the SEPIC is well designed to eliminate the case where the designed compensator cannot offer much due to a poorly designed plant. In this work, the SEPIC converter has been designed using industrial best practices and systematic methodology. The SEPIC converter has been designed following the AN-1484 and TPS-61175 design guides from Texas Instruments (TI). The final design of the converter was tuned to accommodate and withstand the severe tests, as will be explained in later sections. The final design of the designed SEPIC converter is shown in **Table 1**.

Table 1. Designed SEPIC circuit parameters.

Inductor L1, L2	Capacitor C1	Capacitor C2	Load	Input voltage	Output voltage/power	Switching frequency
0.25 mH	2.78 uF	23.15 uF	46.08 Ω	24 V	48 V/50 W	50 kHz

4. Linear and nonlinear controller overview and design for SEPIC converter

4.1. Linear controller

Linear compensators in power converters are designed based on negative feedback systems. The definition of a negative feedback system dictates that the

relationship between the output and the input must be maintained despite the change in the amplitude as well as the rate of change in the control variable, even in the presence of perturbations in the system. Negative feedback is achieved by introducing a new block to the system that takes the error between the output and the set point as its input. This block is referred to as a compensator (other references refer to it as a controller) because it compensates for system imperfections by tailoring the response of the system [9]. Linear compensators can be presented in different structures, such as PID, lead/lag compensators, state feedback, Type-I, -II, -III compensators, etc. In this work, a Type-II compensator and an integral LQR controller were studied. Type-II compensator is standard in the power converter field, and it forms the benchmark for comparative analysis, while an integral LQR controller forms the optimized version of the linear controllers. In the next subsections, Type-II compensators will be discussed. After that, the following subsections will address the integral LQR system.

Type-II compensator:

The Type-II compensator transfer function is comprised of two poles and one zero. It is designed by placing one pole at the origin while the remaining zero-pole pair is placed at a desired/designed location. The placement of the zero-pole pair creates a region of zero gain slope and a corresponding boost in the phase, as shown in **Figure 4**.

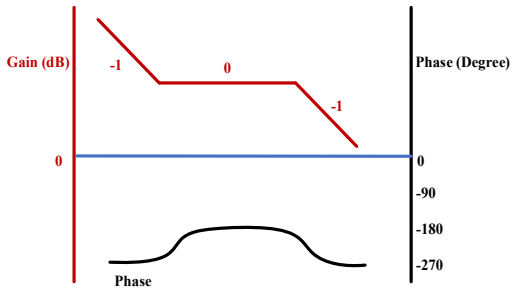


Figure 4. Plot of Type-II transfer function.

This compensator boosts the phase shift from −270° towards −180° during the zero-slope region. Hence, it is evident from **Figure 4** that the maximum boost in the phase is 90 degrees, while the region of this boost is dependent on the zero-slope region. That is, the location of the zero-pole dictates the region where the phase boost will occur. Typically, a Type-II compensator is designed where the loop gain cross-over frequency is occurring at the center of the zero-slope region. Hence, the Type-II compensator is given as shown in Equation (9):

$$\boldsymbol{G_c(s) = \frac{K_c}{s}\frac{(1+\frac{s}{w_z})}{(1+\frac{s}{w_p})}} \tag{9}$$

where K_c is a DC gain. It should be noted that the zero should be placed before the poles (i.e., $w_z < w_p$) which implies that the zero is earlier than the pole, hence it satisfies the boost in the phase requirements.

In the literature, there are different approaches to designing Type-*i* compensators (where *i* = I, II, or III). In this work, *K*-factor method will be used as it is a popular approach in the industry as well as it is a systematic procedure. As per the analysis of

the *K*-factor method, the Type-II compensator is the most suitable compensator for the designed SEPIC model in this work.

As per K-factor method, the first step is to select the desired system cross over frequency (w_c) where the transfer function defined in Equation (8) is used to fulfill this task. In the industry, the desired bandwidth is selected to be one-tenth the switching frequency ($\frac{1}{10} f_{sw}$) as per best practices. However, in the existence of RHPZ, this criterion is not a trivial goal to achieve. Equivalently, as per best practices, once the previous criterion is not achieved, the bandwidth is limited to one-tenth of the lowest RHPZ frequencies, such that the design will offer enough margin to suppress the effect of the RHPZ in a closed loop. By investigating the system frequency response as shown in **Figure 5**, the desired system cross-over frequency is located at 445.15 Hz.

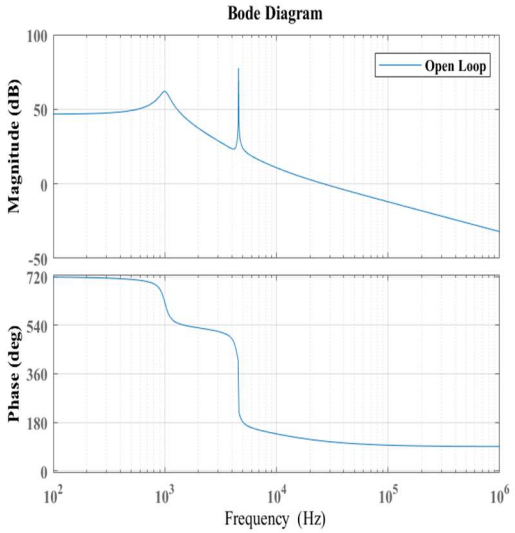


Figure 5. Frequency response of open loop SEPIC converter.

By considering the desired phase margin to be 60°, the required boost in the phase becomes 21°. Therefore, referencing **Table 2**, the needed compensator to use is a Type-II compensator.

Table 2. Compensator type selection guide.

$\boldsymbol{\varphi_{boost} = \text{Phase Margin}_{\text{desired}} - \varphi_{sys} - 90^{\circ}}$	
Required $\boldsymbol{\varphi_{boost}}$	**Compensator type**
Zero degree (**0°**)	Type-I
Less than **90°** (Required $\boldsymbol{\varphi_{boost} < 90°}$)	Type-II
Greater than **90°** (Required $\boldsymbol{\varphi_{boost} \geq 90°}$)	Type-III

After deciding the compensator type, the next step is to start designing the controller parameters. Recalling that Type-II compensator is given by:

$$G_c(s) = \frac{K_c}{s} \frac{(1 + \frac{s}{w_z})}{(1 + \frac{s}{w_p})} \tag{10}$$

The first step will be to calculate w_z and w_p where they are given as:

$$\begin{gathered} \boldsymbol{w_z = \frac{w_c}{K}} \\ w_p = \mathrm{K}.w_c \end{gathered} \tag{11}$$

and K is defined for Type-II compensator to be:

$$K = \tan\left(\frac{\varphi_{boost}}{2} + 45°\right) \tag{12}$$

While determining the type of the compensator the required phase boost is 21°. Hence, the K-factor term will be given as 0.6857. Consequently, the compensator zeros and poles are given as:

$$\begin{gathered} \boldsymbol{w_z = 4.0789 \times 10^3} \text{ Hz} \\ w_p = 1.9179 \times 10^3 \text{ Hz} \end{gathered} \tag{13}$$

Consequently, Type-II compensator for the SEPIC converter demonstrated in **Table 1** is derived to be:

$$G(s)_{comp} = \frac{5997s + 7.823 \times 10^6}{4079s^2 + 7.823 \times 10^6 s} \tag{14}$$

The open loop, loop gain, and the closed loop Bode plots are shown in **Figure 6**.

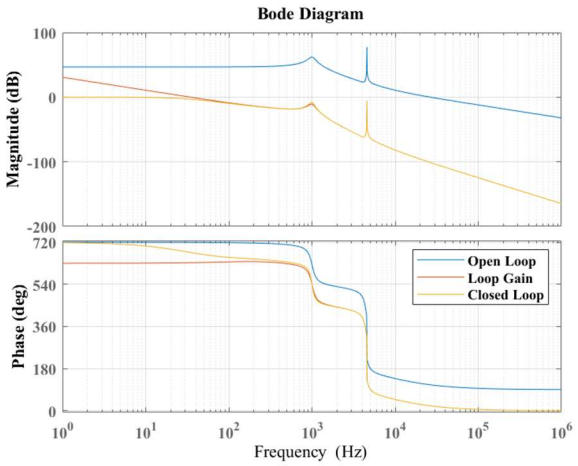


Figure 6. Bode plots of open loop, loop gain, and closed loop.

Integral LQR controller:

Linear quadrature regulator (LQR) is an optimal linear controller that is based on a structural approach to calculate and define the state feedback gains of the system controller. Optimal controllers generally and LQR controllers specifically are based on minimizing a performance index (typically referred to as a cost function) such as the integral of square error denoted by, as given in Equation (15):

$$J = \int_0^\infty (x^T Q x + u^T R u)\mathrm{d}\tau \tag{15}$$

where: x is the state variable vector, u is the control input vector, and Q is a positive semi-definite or definite Hermitian matrix. Q is $n \times n$, where n is number of states, R is a positive definite Hermitian matrix, and R is $r \times r$ where r is the number of inputs.

The performance index proposed in Equation (15) is minimized by solving the Riccati equation as defined in Equation (16):

$$\boldsymbol{A^T P + PA - PBR^{-1}B^T P + Q = 0} \tag{16}$$

where: A is the system matrix, B is the input matrix, Q and R as defined in Equation (15), and P is a positive definite matrix of size $(n \times n)$.

As it can be observed from the Riccati equation, solving the system will result in matrix P since the other variables are either known or assumed without loss of generality. Satisfying the Riccati equation will minimize the cost function, and for the regulator controller case it can be proven that the state feedback gain will be given as:

$$\boldsymbol{K_{gain} = R^{-1}B^{T}P} \tag{17}$$

where: K_{gain} is the state feedback vector.

In some designs, especially in high-order systems, the state feedback controller is not sufficient to perform the tracking task, and it is not capable of rejecting external disturbances, overcoming model uncertainties, or maintaining zero steady-state error. Introducing an integrator usually overcomes these challenges. The integral LQR controller is based on introducing an additional pole at the origin in addition to solving the optimal performance equation. By introducing an integrator to the system, the plant block diagram is depicted in **Figure 7**.

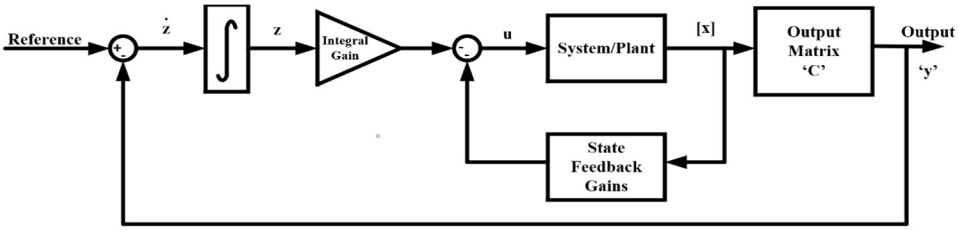


Figure 7. Block diagram of plant with integral LQR.

From **Figure 7**, the new system model with the inclusion of integral action can be described in matrix form to be:

$$\begin{bmatrix} \dot{\boldsymbol{x}} \\ \dot{\boldsymbol{z}} \end{bmatrix} = \begin{bmatrix} \boldsymbol{A} & \boldsymbol{0} \\ -\boldsymbol{C} & \boldsymbol{0} \end{bmatrix} \begin{bmatrix} \boldsymbol{x} \\ \boldsymbol{z} \end{bmatrix} + \begin{bmatrix} \boldsymbol{B} \\ -\boldsymbol{D} \end{bmatrix} \boldsymbol{u} + \begin{bmatrix} \boldsymbol{0} \\ \boldsymbol{1} \end{bmatrix} \boldsymbol{Ref}$$
$$\boldsymbol{y} = [\boldsymbol{C}\ \boldsymbol{0}] \begin{bmatrix} \boldsymbol{x} \\ \boldsymbol{z} \end{bmatrix} + \boldsymbol{Du} \tag{18}$$

Therefore, the model in augmented notion can be described to be:

$$\boldsymbol{\dot{X}_A = A_A X_A + B_A u + FRef}$$
$$\boldsymbol{y = C_A X_A + D_A u}$$

where: $A_A = \begin{bmatrix} A & 0 \\ -C & 0 \end{bmatrix}, B_A = \begin{bmatrix} B \\ -D \end{bmatrix}, C_A = [C\ 0], D_A = D, X_A = \begin{bmatrix} x \\ z \end{bmatrix}$, and $u = -K_A X_A$, where $K_A = [K\ K_i]$.

The following step in designing the integral LQR controller is to define Q and R matrices given in Equation (15), where the Q matrix is required to be positive semi-definite and its dimension is same as (A_A).

Considering the dimension of the SEPIC model, the Q matrix is (5×5) a diagonal matrix, where the *i*-th diagonal element will represent the importance (weight) of the corresponding state variable with respect to the controller objective. In this work, a single input-single output (SISO) structure is adopted to control the SEPIC. As a result, the *R*-matrix will be single value (1×1). The weight of the *R*-element will be the highest because it must be fast to accommodate the switching of the PWM signal generator, provide an acceptable transient response, and provide comparable performance with respect to nonlinear techniques. The elements of the Q

and *R* matrices are tuned to achieve the desired performance.

The next step is to derive and solve the Riccati equation of the integral LQR. In this work, the optimization is done using the MATLAB toolbox to tune the Q and R matrices and obtain the desired response, while the cost and the state feedback gains are optimized using the MATLAB toolbox tools. The integral LQR controller was designed and tuned for the designed SEPIC converter, as shown in **Table 1**. Using MATLAB simulation to solve the optimization problem, the designed controller gains are listed in **Table 3**.

Table 3. Summary for the designed gains for Integral LQR controller.

Gain 1—K_1	Gain 2—K_2	Gain 3—K_3	Gain 4—K_4	Gain 5—K_5
0.00659	0.00375	−1.60361	0.000385	−3.87298

4.2. Review of sliding mode controller, equivalent control law derivation, and modulation techniques

A sliding mode controller (SMC) is a variable-structure controller. The SMC provides robust tracking for a desired trajectory by defining a sub-manifold that includes the desired trajectory. This manifold is defined as a sliding surface. The construction of the sliding surface is not unique; however, any sliding surface must satisfy the following conditions:

1) The derivative of the sliding surface must include the control input explicitly.
2) As the surface is approaching a zero state, the tracking of the desired trajectory must be achieved.

Typically, the sliding surface can be constructed using a linear combination of the state error functions, linear/nonlinear combinations of the state variable, and an integral or derivative of the aforementioned combinations.

Before deriving the control law for the proposed SMC, a brief explanation of the sliding surface dynamics is provided.

Consider the nonlinear *n*-th-order system:

$$x^n = f(X,t) + b(X,t).u(X,t) + d(t),$$

where:

- $f(X,t)$ is the nonlinear system model (it may not be exactly known) which must be bounded from above by a known continuous function of the state variable (X) and time (t),
- $b(X,t)$ is the control gain which must also be bounded by a constant function of state variable (X) and time (t),
- $u(X,t)$ is the control input, and
- $d(t)$, is unknown and must be bounded from above by a known continuous function of the state variable (X) and time (t).

It can be shown that the SMC successfully tackles the highly nonlinear and bilinear system, which makes it a perfect candidate for power converters.

If the sliding surface is constructed to include the desired trajectory, then solving the control problem will require two actions:

1) Reaching the sliding surface from any point in the space (regardless of the initial conditions), and

2) Staying on the surface at the desired state.

The first action, reaching the sliding surface, can be achieved by satisfying the sliding condition which is defined to be:

$$\frac{1}{2}\frac{d}{dt}\mathbb{S}^2 \leq -\eta|\mathbb{S}| \tag{19}$$

where $\mathbb{S}$ is sliding surface and η is a positive constant.

If the sliding condition in Equation (19) is satisfied, this will imply that the squared distance towards the surface will keep decreasing, which will force the trajectories to converge towards the sliding surface regardless of the presence of disturbances and the imprecisions in the modeled dynamics. Further, the sliding condition ensures that the sliding surface will be reached, regardless of the initial condition, in a finite time given by:

$$time_{reach\ surface} \leq \frac{\mathbb{S}(t=0)}{\eta}. \tag{20}$$

Furthermore, satisfying the sliding conditions will make the time-varying surface an invariant set. In other words, the surface as $\mathbb{S}^2$ must be maintained as a Lyapunov function with respect to the defined control law.

The second required action to define proper constraints to derive the control law is to ensure that the system will stay on the sliding surface after reaching it. In other words, if the control law is derived such that the sliding surface that is defined for the system's dynamical equations leads to a zero value, then this implies that the desired states reside on the surface; hence, the first derivative must be zero. **Figure 8** illustrates this aspect of the sliding mode controller.

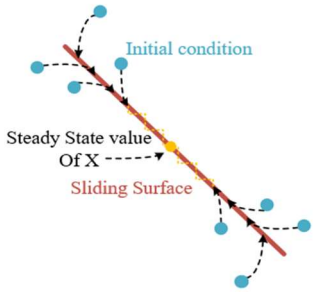


Figure 8. Illustrative trajectory on a sliding surface.

Equivalent control law derivation:

To derive the control law of the SMC, the first step requires constructing the sliding surface based on the earlier discussion. The second step is to define the control law to be:

$$u = u_{eq} + u_n \tag{21}$$

where u_{eq} is the equivalent control vector, while u_n is the switching control term.

The equivalent control term (u_{eq}) is a continuous term, and it is derived based on the system dynamics that will ensure the rate of change in the sliding surface is zero. Typically, the equivalent control term is derived as follows:

1) Find the derivative of the constructed sliding surface,
2) Equate the obtained derivate to zero, and
3) Solve for the control term.

On the other hand, the second term is the switching control term (u_n) which is discontinuous; it accounts for the uncertainties and the system disturbances. Typically, the switching control is given by:

$$u_n = -K_{slide} sgn(\mathbb{S}),$$

where K_{slide} is a positive constant, $\mathbb{S}$ is the sliding surface and sgn is the sign function which is described as:

$$sgn(s) = \begin{cases} 1 \text{ if } \mathbb{S} > 0 \\ -1 \text{ if } \mathbb{S} < 0 \end{cases}$$

The role of $\mathbb{S}$ is to provide enough correction to compensate for any uncertainty or disturbance, while the sign function will ensure the trajectory to the correct direction.

The overall control term (including the equivalent and the switching) can be summarized in the next steps:

1) Find the derivative of the sliding surface ($\dot{\mathbb{S}}$).
2) Equate the ($\dot{\mathbb{S}}$) surface with the switching control term:

$$\dot{\mathbb{S}} = -K_{slide} sgn(\mathbb{S}).$$

3) Solve for the control input term u.

The major advantage of this approach is that it ensures the inclusion of the input vector over the switching control term; hence, the controller will be able to perform a better task in the tracking requirements.

Modulation techniques of the SMC:

In the literature, the SMC is implemented by using either of the following approaches:

- Hysteresis modulation (HM) controller,
- PWM-based on equivalent control law.

a. The hysteresis modulation (HM) controller:

This technique of implementing the SMC is based on the instantaneous sign of the sliding surface, which is defined with respect to the trajectory. Unlike the control law discussed in Equation (21), the HM Controller's control law is simpler and is defined as:

$$\boldsymbol{u = \frac{1}{2}\left(1 - sgn(\mathbb{S})\right) = \begin{cases} u^+ \ \mathbb{S} < 0 \\ u^- \ \mathbb{S} > 0 \end{cases}} \quad (22)$$

Intuitively, the system follows the Filipov structure, where the control signal is composed of two components; each component will guide the system in a region based on the sign of the region with respect to the sliding surface given that the sliding is defined to be zero ($\mathbb{S} = 0$), as illustrated in **Figure 9**.

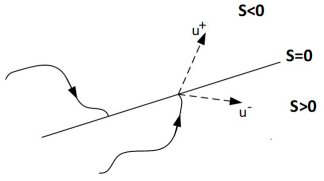


Figure 9. Control law structure using hysteresis controller.

In power converters, the control signal can be either 1 or 0 to drive the semiconductor switch. Therefore, the HM controller will be given as:

$$\boldsymbol{u} = \frac{\mathbf{1}}{\mathbf{2}}\left(\mathbf{1} - \boldsymbol{sgn}(\mathbb{S})\right) = \begin{cases} \mathbf{1} & \mathbb{S} < \mathbf{0} \\ \mathbf{0} & \mathbb{S} > \mathbf{0} \end{cases} \quad (23)$$

To satisfy the relationship in Equation (23), the reachability condition for the sliding condition must be met. Hence, by defining a proper Lyapunov candidate function such as ($V = \frac{1}{2}\mathbb{S}^2$), the stability can be proven by having ($\dot{V} = \mathbb{S}\dot{\mathbb{S}} < 0$) which matches with the reachability condition. Consequently, reachability and stability are totally dependent on the sliding surface to satisfy the Lyapunov theorem.

Adopting the HM controller to generate the control signal for SMC suffers from several drawbacks. Firstly, the structure requires infinite switching frequency because it reacts based on the instantaneous sign of the sliding surface. Introducing such a high frequency will introduce high noise in the circuit. Further, the practical implementation of such high-frequency switching is a challenge, and having a sluggish switching behaviour will result in poor performance. On the other hand, if the system requires an input or output filter, then the overall design will be oversized and complicated to satisfy the frequency range of operation. One of the techniques to limit the infinite frequency requirement is to make the switching with respect to a small threshold instead of zero. In other words, the HM controller will be defined as:

$$\boldsymbol{u} = \frac{\mathbf{1}}{\mathbf{2}}\left(\mathbf{1} - \boldsymbol{sgn}(\mathbb{S})\right) = \begin{cases} \mathbf{1} & \mathbb{S} < \boldsymbol{\epsilon} \\ \mathbf{0} & \mathbb{S} > -\boldsymbol{\epsilon} \end{cases} \quad (23)$$

It is highlighted that the introduction of the delay limits the frequency; however, the frequency is still a variable. Furthermore, the value of ϵ is determined by tuning.

b. PWM-based on equivalent control law:

Unlike the HM controller, the PWM-based controller operates at a fixed frequency. Hence, it overcomes all the aforementioned cons. On the other hand, an additional yet simple circuit will be needed to generate the PWM signal. Typically, the PWM signal is generated by comparing a fixed-frequency sawtooth or triangular signal with a reference value. In a power converter, the entered reference signal is the duty cycle of the switch. The comparator will operate the switch by on/off pulses at a fixed frequency.

In SMC implementation, the duty cycle is obtained from the equivalent control law that was illustrated earlier. Typically, the rate of change on the sliding surface is equal to zero. Then, by the definition of the sliding surface, the equation can be solved for a closed form of the control law. In other words:

$$\dot{\mathbb{S}} = 0 \rightarrow \text{solve } f \text{or } u$$

The equivalent control law, as discussed earlier, is continuous and smooth, and it represents the duty cycle of the converter. In other words, the equivalent control signal has low-frequency components and is chatter-free. Therefore, it is a proper representation of the duty cycle of the power converter.

By comparing the generated equivalent control signal to a sawtooth or a triangular signal, the PWM signal is generated to drive the semiconductor switch. One of the disadvantages of this type of technique is that it is weak in its ability to reject disturbances and account for uncertainty. This is because the high-frequency components (switching signals) are not included in the control law. Generally, adding the switching may lead to high chattering in the generated control law and will make the task of generating proper PWM at a fixed frequency imprecise. Nevertheless,

constructing a proper sliding surface based on understanding the model dynamics employs the switching signal, such as the sign function, effectively where the chattering is minimal, and the system is robust with high capability to reject disturbances, uncertainties, and unmodeled dynamics.

5. Derivation of the proposed controller and step-by-step design guide

In this work, a novel approach is proposed to generate the control signal using PWM techniques. The procedure starts by constructing a stable and simple sliding surface. Then the equivalent control law is derived and scaled; a method to define a valid value for the associated gain is introduced. The next step is to add the switching control signal with a proper scaling coefficient. The gain values (for the equivalent and switching controller) are selected to ensure that the chattering is minimal in the converter output as well as in the generated duty cycle; moreover, the gain values are selected to ensure the converter is highly robust against unmodeled dynamics, system uncertainties, and external disturbances.

Typically, the SMC with an equivalent controller approach suppresses the switching element (high frequency) at the cost of system robustness, as discussed earlier. To overcome this scenario and to include the switching element, both the equivalent controller and the switching control signal will be scaled with a proper gain. In the last stage, the total control signal as defined in Equation (21) is used as the input to the PWM generator block. The generated pulses out of the PWM block will be at a fixed frequency, and they will drive the switch in the converter.

Derivation of the sliding surface

Several researchers have discussed SMC for the SEPIC converter and the construction of appropriate sliding surfaces, such as in the studies of Aroudi et al. [6] and Deisch et al. [7]. Depending on the system requirements, combinations of the state variables can be used to construct the surface. In most of the applications described in the literature, the control target is to achieve a robust output voltage tracking task. Hence, it would be expected that the sliding surface will be written as a scaled error function of the output voltage, an integral of the output voltage error signal, or a linear or nonlinear combination of the error signal and its integral. However, this approach is effective for Ćuk converters but not for SEPIC converters. Although both Ćuk and SEPIC are fourth-order converters, they have fundamentally different structures. The studies of Zhang et al. [14] and Hamed et al. [15] have shown that the stability of a sliding surface can be achieved by the earlier discussed approach; in fact, they proved the instability of the surface if it was constructed only by any combination form of output voltage, whether error signal, integral form, or even derivative form. This cited research has shown that to have a stable surface, the surface must include at least one inductor current in the sliding manifold. Nevertheless, there was no concrete justification for the reason behind the inclusion of a state variable such as an inductor current to stabilize the surface.

The answer behind the stabilization of the sliding surface upon the inclusion of the inductor currents relies on investigating the small signal approximation in the

transfer function form. By analyzing the transfer function of the system, where the input is the duty cycle and the output is the inductor current, it is evident that the system is a minimum phase with poles in the left-hand plane (stable system). On the other hand, once the transfer function of SEPIC is constructed between the duty cycle and the output voltage, the resulting system has a non-minimum phase. For this reason, the sliding surface must be constructed to control the output voltage indirectly by introducing the inductor current into the surface. For instance, for the designed converter in this work, the zeros of the SEPIC transfer function from the duty cycle to the input inductor current are given as $-2444 \pm 30{,}817j$ and -1883 which confirms that the system is in the minimum phase due to the zero placement in the left-hand plane region.

As a result, let the sliding surface to be:

$$\mathbb{S} = \boldsymbol{i_{L1}} + \boldsymbol{\lambda} \int (\boldsymbol{v_{C2}} - \boldsymbol{v_{ref}}) \mathbf{d}\boldsymbol{\tau} \tag{25}$$

where λ is a positive constant that is designed as follows:

(1) First, the equivalent control law is derived as discussed in previous sections:

- Find the derivative of the constructed sliding surface and equate the obtained derivate with zero:

$$\frac{\mathbf{d}\boldsymbol{s}}{\mathbf{d}\boldsymbol{t}} = \dot{\mathbb{S}} = \frac{\boldsymbol{d}}{\mathbf{d}\boldsymbol{t}}\left(\boldsymbol{i_{L1}} + \boldsymbol{\lambda} \int (\boldsymbol{v_{C2}} - \boldsymbol{v_{ref}}) \mathbf{d}\boldsymbol{\tau}\right) = \mathbf{0}$$

$$\dot{\mathbb{S}} = \dot{\boldsymbol{\iota}}_{\boldsymbol{L1}} + \boldsymbol{\lambda}(\boldsymbol{v_{C2}} - \boldsymbol{v_{ref}}) = \mathbf{0} \tag{26}$$

$$\dot{\mathbb{S}} = -\frac{\boldsymbol{r_{L1}}}{\boldsymbol{L_1}} \boldsymbol{i_{L1}} + \frac{\boldsymbol{u} - \mathbf{1}}{\boldsymbol{L_1}} \boldsymbol{v_{C1}} + \frac{\boldsymbol{u} - \mathbf{1}}{\boldsymbol{L_1}} \boldsymbol{v_{C2}} + \frac{\boldsymbol{v_g}}{\boldsymbol{L_1}} + \boldsymbol{\lambda}\left(\boldsymbol{v_{C2}} - \boldsymbol{v_{ref}}\right) = \mathbf{0}$$

- Solve for the control term:

$$\boldsymbol{u_{eq}} = \frac{\left[\boldsymbol{r_{L1}} \boldsymbol{i_{L1}} + \boldsymbol{v_{C1}} + \boldsymbol{v_{C2}} - \boldsymbol{v_g} - \boldsymbol{\lambda} \boldsymbol{L_1}\left(\boldsymbol{v_{C2}} - \boldsymbol{v_{ref}}\right)\right]}{\boldsymbol{v_{C1}} + \boldsymbol{v_{C2}}} \tag{27}$$

(2) Since the control signal is needed to operate the switch in the SEPIC, u_{eq} is bounded by the limits of the PWM signals that turn on/off the semiconductor switch. In other words, u_{eq} is bounded between 0 and 1; that is:

$$0 < u_{eq} < 1$$

By applying the lower and upper bounds of u_{eq} (i.e., the zero and one respectively), the corresponding domain of λ can be defined. For simplicity, the ideal model will be described here, where the parasitic value is suppressed.

Consider the lower bound: ($u_{eq} > 0$)

$$\frac{\left[\boldsymbol{v_{C1}} + \boldsymbol{v_{C2}} - \boldsymbol{v_g} - \boldsymbol{\lambda} \boldsymbol{L_1}\left(\boldsymbol{v_{C2}} - \boldsymbol{v_{ref}}\right)\right]}{\boldsymbol{v_{C1}} + \boldsymbol{v_{C2}}} > \mathbf{0} \tag{28}$$

Then, the inequality can be described as:

$$\left[\boldsymbol{v_{C1}} + \boldsymbol{v_{C2}} - \boldsymbol{v_g} - \boldsymbol{\lambda} \boldsymbol{L_1}\left(\boldsymbol{v_{C2}} - \boldsymbol{v_{ref}}\right)\right] > \mathbf{0} \tag{29}$$

By solving for $\boldsymbol{\lambda}$, the following inequality is obtained:

$$\boldsymbol{\lambda} < \frac{\mathbf{1}}{\boldsymbol{L_1}}\left(\frac{\boldsymbol{v_g} - \boldsymbol{v_{C1}} - \boldsymbol{v_{C2}}}{\boldsymbol{v_{ref}} - \boldsymbol{v_{C2}}}\right) \tag{30}$$

The next step, is to consider the upper bound: ($u_{eq} < 1$)

$$\frac{\left[\boldsymbol{v_{C1}} + \boldsymbol{v_{C2}} - \boldsymbol{v_g} - \boldsymbol{\lambda}.\boldsymbol{L_1}\left(\boldsymbol{v_{C2}} - \boldsymbol{v_{ref}}\right)\right]}{\boldsymbol{v_{C1}} + \boldsymbol{v_{C2}}} < \mathbf{1} \tag{31}$$

The inequality, can be simplified to be:

$$\boldsymbol{\lambda < \frac{1}{L_1}\left(\frac{v_g}{v_{ref} - v_{C2}}\right)} \tag{32}$$

When comparing the two results from the inequalities in Equations (30) and (32), the result of the inequality in Equation (32) will be used, as this constraint also satisfies the inequality in Equation (30). The maximum value of λ is described by inequality Equation (32) and will be achieved once $v_{C2} = 0$. It should be noted that the SEPIC is operated in continuous conduction mode (CCM) with a positive input voltage; thus v_{C2} is positive.

Next, λ must be selected to satisfy the bounds:

$$\boldsymbol{0 < \lambda < \frac{1}{L_1}\left(\frac{v_g}{v_{ref}}\right)} \tag{33}$$

By defining and deriving all the parameters on the sliding surface, the next task will be to derive the sliding mode controller law. This is achieved by following the steps in the aforementioned sections; the sliding mode controller is derived as follows:

(1) Find the derivative of the sliding surface ($\dot{\mathbb{S}}$):

$$\boldsymbol{\frac{ds}{dt} = \dot{\mathbb{S}} = \frac{d}{dt}\left(i_{L1} + \lambda \int (v_{C2} - v_{ref})d\tau\right)}$$

$$\boldsymbol{\dot{\mathbb{S}} = \dot{\imath_{L1}} + \lambda(v_{C2} - v_{ref})} \tag{34}$$

$$\boldsymbol{\dot{\mathbb{S}} = -\frac{r_{L1}}{L_1} i_{L1} + \frac{u-1}{L_1} v_{C1} + \frac{u-1}{L_1} v_{C2} + \frac{v_g}{L_1} + \lambda\left(v_{C2} - v_{ref}\right)}$$

(2) Equate the ($\dot{\mathbb{S}}$) with the switching control term:

$$\boldsymbol{\dot{\mathbb{S}} = -K_{slide} sgn(\mathbb{S})}$$

$$\boldsymbol{-\frac{r_{L1}}{L_1} i_{L1} + \frac{u-1}{L_1} v_{C1} + \frac{u-1}{L_1} v_{C2} + \frac{v_g}{L_1} + \lambda\left(v_{C2} - v_{ref}\right) = -K_{slide} sgn(\mathbb{S}),} \tag{35}$$

where K_{slide} is positive constant, and s is the sliding surface.

(3) Solve for the control input term u:

$$\boldsymbol{u = \frac{\left[r_{L1} i_{L1} + v_{C1} + v_{C2} - v_g - \lambda L_1\left(v_{C2} - v_{ref}\right) - K_{slide} L_1 sgn(\mathbb{S})\right]}{v_{C1} + v_{C2}}} \tag{36}$$

where:

- λ is selected to satisfy the inequality given in Equation (33),
- $\mathbb{S}$ is the sliding surface defined in Equation (25), and
- K_{slide} is a positive constant.

The last step is to tune λ and K_{slide} to provide the desired responses in terms of zero steady state error, disturbance rejection and uncertainty compensation, and to ensure the least chattering in the output as well as in the duty cycle.

6. Stability analysis of the proposed controller

The stability analysis of the system is evaluated by studying the Lyapunov candidate function:

$$\boldsymbol{V = \frac{1}{2}\mathbb{S}^2} \tag{37}$$

where V is the Lyapunov function and $\mathbb{S}$ is the sliding surface. The selected Lyapunov function is positive definite.

By taking the derivative of the Lyapunov function:

$$\dot{\boldsymbol{V}} = \mathbb{S}\dot{\mathbb{S}} \tag{38}$$

In a similar proof to the stability of the Lyapunov function, the system stability is proved if the Lyapunov function is positive definite and its derivative is negative definite. Substituting the expressions of the derivative of the sliding surface, we can get:

$$\dot{\boldsymbol{V}} = (\mathbb{S}).\left(-\frac{\boldsymbol{r_{L1}}}{\boldsymbol{L_1}}\boldsymbol{i_{L1}} + \frac{\boldsymbol{u-1}}{\boldsymbol{L_1}}\boldsymbol{v_{C1}} + \frac{\boldsymbol{u-1}}{\boldsymbol{L_1}}\boldsymbol{v_{C2}} + \frac{\boldsymbol{v_g}}{\boldsymbol{L_1}} + \boldsymbol{\lambda}\left(\boldsymbol{v_{C2}} - \boldsymbol{v_{ref}}\right)\right) \tag{39}$$

The controller derived in Equation (36) will be substituted into the expression in Equation (39). The final expression is given as:

$$\dot{\boldsymbol{V}} = (\mathbb{S})\left(-\frac{\boldsymbol{K_{slide}}}{\boldsymbol{L_1}}\boldsymbol{sgn}(\mathbb{S})\right) = -\frac{\boldsymbol{K_{slide}}}{\boldsymbol{L_1}}|\mathbb{S}| \tag{40}$$

The result in Equation (40) states that the derivative of the Lyapunov function ($\dot{V}$) is negative definite which proves that the system is globally asymptotically stable.

This result can be visualized by recalling the reachability condition:

$$\frac{1}{2}\frac{d}{dt}\mathbb{S}^2 \leq -\eta|\mathbb{S}|$$

The expression can be simplified to be:

$$\mathbb{S}\dot{\mathbb{S}} \leq -\eta|\mathbb{S}|$$

By carrying the same previous steps of substituting the derived control law in $\dot{\mathbb{S}}$, we get the following result:

$$-\frac{K}{L_1}|\mathbb{S}| \leq -\eta|\mathbb{S}|$$

Thus, by proper assignment of η, the reachability to the sliding surface is ensured and the convergence rate will be given as:

$$time_{\text{reach surface}} \leq \frac{\mathbb{S}(t=0)}{\eta}$$

Hence, by proving that the rate of change in the surface is negative definite, then the system is globally asymptotically stable.

7. Results

7.1. Simulation results: Type II compensator, integral LQR, proposed controller

Simulating the designed controller and assessing its dynamic behaviour is an essential step before experimentally implementing and testing the developed controller. A MATLAB/Simulink simulation was conducted with the switched nonlinear model rather than an averaged model as an essential first step to validate a model that is as close as possible to a practical scenario. The simulation results were generated for the SEPIC converter using the parameters given in **Table 1**. The comparative evaluation and the analysis cover the three discussed controllers: (a) Type-II compensator, (b) integral LQR, and (c) the proposed ISMC. For all three controllers, the following three test conditions were applied: Cold start-from-rest test, input voltage disturbance test, and load disturbance test.

Converter start-from-rest test:

This test investigates the output voltage of the converter when all the initial conditions are at rest (assumed to be zero). The test results for the three compensators are shown in **Figure 10(a–c)** for the output voltage of the SEPIC converter and **Figure 11(a–c)** for the converter duty cycle, respectively.

a) The Type-II compensator controller resulted in an overdamped response and achieved the tracking task with zero steady-state error with a settling time of 40 ms, as shown in **Figure 10(a)**. **Figure 11(a)** shows the corresponding generated duty cycle by the compensator, and it is evident that it does not have a high ripple. This result is critical to validating the design and moving it from a simulation environment to an experimental model.

b) The integral LQR compensator resulted in a response where the output voltage reached the steady state in a settling time of 10 ms. **Figure 10(b)** shows that the designed compensator resulted in making the system reach the steady state with an overdamped response and perform the tracking task with zero steady-state error. **Figure 11(b)** shows the corresponding generated duty cycle by the compensator where it has a low ripple, and this result is critical in validating the designed controller.

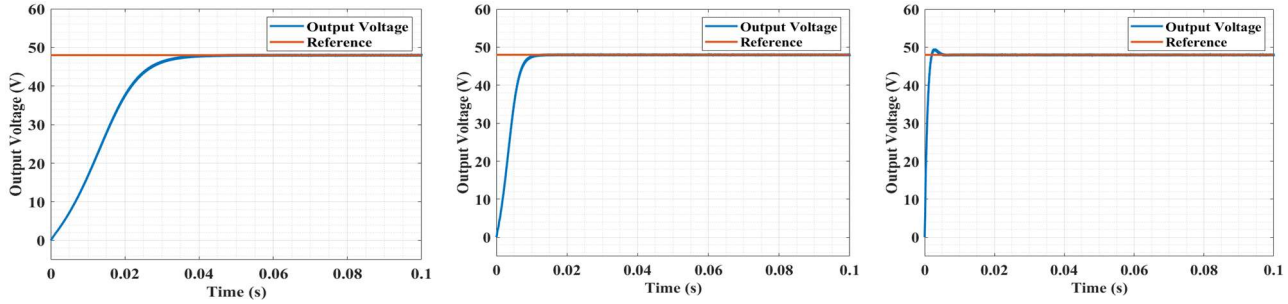


Figure 10. Converter's output voltage at cold start test **(a)** Type-II; **(b)** integral LQR; **(c)** proposed ISMC.

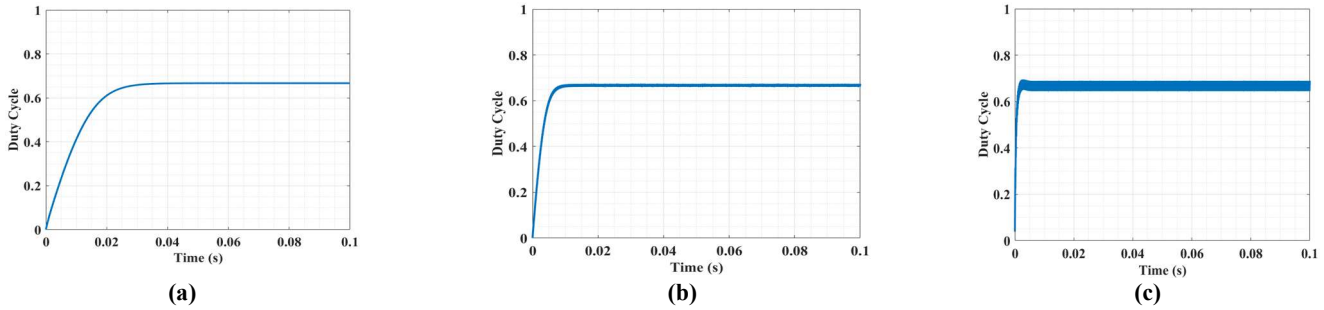


Figure 11. Converter's duty cycle at cold start test **(a)** Type-II; **(b)** integral LQR; **(c)** proposed ISMC.

c) The results of the proposed ISMC controller under the cold start test are depicted in **Figures 10(c)** and **11(c)**. The results show that the converter output voltage reaches the desired output level in 5 ms, and the transient shows a minor overshoot that peaked at 49.6 V (3.3% overshoot). Moreover, the converter using the proposed controller can perform the tracking task with zero steady-state error in the output voltage. Additionally, **Figure 10(c)** shows that after reaching the steady state, the converter output voltage is stable with minimum chattering.

These results are achieved because of the advantages of the proposed ISMC sliding surface, which is based on using the input current (inductor current) and the integral of the output voltage error. The proper design of the surface ensures the system will reach the sliding surface and continue to stay on it. By residing within the sliding surface and sliding on it, the desired point will always be reached. This process ensures smooth transients and reduced chatter in the converter's duty cycle D at steady state, as shown in **Figure 11(c)**. This is typically relevant in applications where the converter is expected to periodically start and stop. It is noted that the dynamics of the duty cycle reflect the output voltage. As shown in **Figure 11(c)**, the duty cycle reaches a steady state in 5 ms with low chattering. This behaviour is identical to that of the output voltage. In fact, verifying the behaviour of the duty cycle in a DC-DC power converter simulation is essential to proving that the converter and its controller have been well designed and that the output voltage behaviour is adhering to the dictated behaviour of the duty cycle. The aforementioned discussion illustrates the advantages of the proposed controller, as the obtained system response does not need to use soft starting techniques/circuits since the response is faster than the other designed controllers.

In summary, this section highlights the first test, where the converter was tested using the three examined controllers under the cold start condition. The study established the Type-II compensator as a benchmark for the analysis and comparison against the integral LQR and the proposed ISMC controllers. The main challenge in this test is starting from zero initial conditions, i.e., charging the storage elements of the SEPIC converter is part of the dynamics when starting from zero. **Table 4** summarizes the results of the simulated cold start test using the three controllers.

Table 4. Comparison of simulation results for the cold test.

Cold start test			
	Type-II	**Integral LQR**	**Proposed ISMC**
Response	Overdamped	Overdamped	Close to critically damped
Settling time	50 ms	10 ms	5 ms

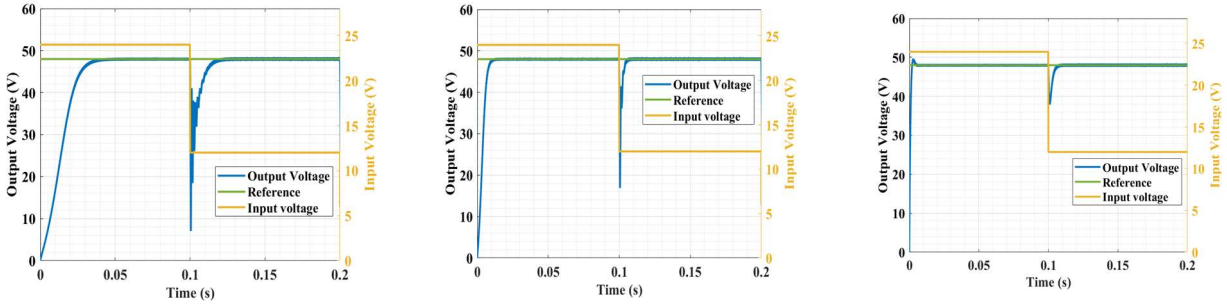
The summarized results state that the Type-II compensator has an overdamped response, and it took 50 ms to reach the steady state. The integral LQR controller had a similar result where the response was overdamped and required only 10 ms to reach steady-state. On the other hand, the proposed controller was much faster, with only a minor overshoot in the output voltage response, and required only 5 ms to reach the steady state. This is 2 times faster than the integral LQR and 10 times faster than the Type-II compensator. During the test, the overshoot reached 49.6 V (3.3% overshoot), given that the input reference is a step function. This overshoot is small, and if the system requires the response to be without an overshoot, then the reference can be adjusted to be a ramped input until the reference reaches the desired level. It should be noted that a ramping reference is a common practice in power electronics to avoid inrush currents in the system. Moreover, the proposed ISMC controller can be tuned easily by re-adjusting the λ value. Hence, if the goal is to achieve a cold start using a step function input without an overshoot, then the designer can reduce the used λ value accordingly until the desired response is achieved.

The depicted results of the cold start test in previous sections showed that the output voltage from the proposed controller has a low ripple like the linear controllers' case. Sliding mode controllers usually suffer from chattering in the output response if a "sign" function is used as part of the controller. This result demonstrates that the design procedure is based on the relationship between the converter states on the newly constructed surface. Furthermore, the scaling gain constant, λ, has been bounded, to ensure system stability with low chattering behaviour. Another point to highlight is the choice of operating the system on a fixed frequency. This reduces the chattering as the converter internally sees an equivalent DC value for the duty cycle D; this makes the converter operate in PWM mode, which effectively results in a low ripple system if the converter components are well-sized.

Input voltage disturbance test:

In this test, the three compensators using the SEPIC converter are evaluated against an input voltage disturbance. Each compensator performance is evaluated in two stages: in the first stage, the converter is subjected to a single disturbance; and in the second stage, the converter is subjected to multiple input voltage disturbances by stepping it down from 24 V to 12 V and then to 6 V. This type of disturbance in the input voltage is considered severe and may be considered out of range for some applications; however, it is of importance in applications where a wide range of input voltages are expected (e.g., different batteries, universal AC input, or use of ultracapacitors). It is noted that the load is kept constant at its nominal value during this test.

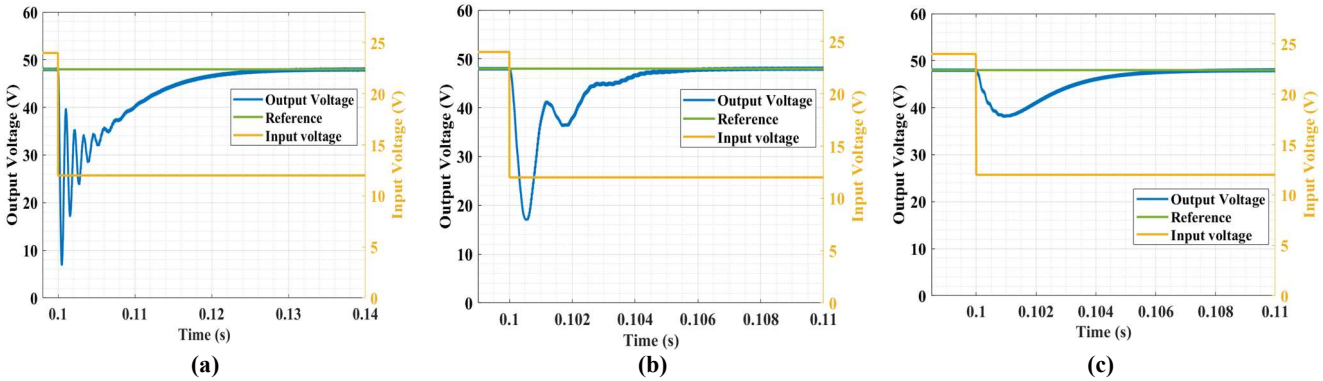
a) For the Type-II compensator, after reaching the steady-state condition, the input voltage is stepped down from 24 V to 12 V at 0.1 s, as shown in **Figures 12(a)** and **13(a)**. In this test, the compensator was able to recover from the disturbance in 25 ms. As shown in the figure, the response suffers from a deep undershoot that dropped to 6.8 V. Furthermore, during the recovery process, the response was oscillatory. By varying the input voltage by 50%, the obtained results are not as desired in the power electronics field, as the response is slow, has a large undershoot, and exhibits a large oscillatory response. In the second stage, the converter is subjected to the same previous disturbance at 0.1 s, then another disturbance is introduced at 0.2 s, where the input voltage is reduced from 12 V to 6 V. As shown in **Figures 14(a)** and **15(a)**, the output voltage in the second disturbance has dropped from 48 V to 11.5 V, and it recovered from the disturbance in 15 ms. As depicted in **Figures 12(a)**–**Figure 15(a)**, the response suffers from a deep undershoot, a sluggish response, and oscillations in the recovery process. During this test, the duty cycle is shown in **Figure 16(a)**. The result shows that the corresponding duty cycle has a low ripple, and it is implementable in the experimental setup. Furthermore, the duty cycle corresponds to the output voltage behaviour, where the compensator takes time to adjust the duty cycle; hence, the sluggish response is justified.



(a) **(b)** **(c)**

Figure 12. Step change in the input voltage from 24 V to 12 V at t = 0.1 s and the corresponding output voltages. **(a)** Type-II compensator; **(b)** integral LQR; **(c)** proposed ISMC.

b) For the integral LQR controller, after reaching the steady-state condition, the input voltage is stepped down from 24 V to 12 V at 0.1 s, as shown in **Figures 12(b)** and **13(b)**. In this test, the compensator was able to recover from the disturbance in 5 ms. As shown in **Figures 14(b)** and **15(b)**, the response had an undershoot with oscillations that dropped as low as 17 V. By comparing the results, it is concluded that the integral LQR controller resulted in a faster response and better undershoot peak; however, the system is still exhibiting an oscillatory behaviour in withstanding the 50% variation in input voltage disturbance. As stated earlier, the disturbance in input voltage will be validated through two cascaded disturbances/ stages. The first-stage results have been depicted in **Figure 12(b)**. In the second stage, first the converter is tested as in case one, then another disturbance is introduced at 0.2 s, where the input voltage is reduced again from 12 V to 6 V. As shown in **Figure 14(b)**, at the first disturbance, the output voltage dropped to 17 V and then recovered from the disturbance in an oscillatory response in 5 ms. The output voltage in the second disturbance dropped from 48 V to 22.5 V, then it showed another overshoot that reached 51.8 V before starting the recovery process. The system, after the second disturbance, reached a steady state again in 7 ms. As depicted in **Figures 12(b)**–**Figure 15(b)**, the response suffers from undershoot, overshoot, and oscillations during the recovery process. During this test, the duty cycle was recorded in **Figure 16(b)**. The result shows that the corresponding duty cycle has a low ripple, and it is implementable experimentally.



(a) **(b)** **(c)**

Figure 13. Zoomed portion during the step change in the input voltage from 24 V to 12 V at t = 0.1 s. **(a)** Type-II compensator; **(b)** integral LQR; **(c)** proposed ISMC.

c) Like Type-II and the integral LQR controller, the proposed ISMC is subjected to multiple input voltage disturbances in the same manner. The test is conducted after waiting for the system to reach the steady-state condition; then, the input voltage is stepped down from 24 V to 12 V at 0.1 s, as shown in **Figure 12(c)**. The zoomed portion of the response is shown in **Figure 13(c)**. The proposed ISMC provides a smooth, damped transient without oscillation in 6 ms, while the maximum undershoot peak reaches 38.5 V. By observing the ripple on the output voltage, the ripple increased by 0.2% after disturbing the input voltage by 50% from its initial value. In **Figures 14(c)** and **15(c)**, at $t = 0.2$ s, the input voltage is once again stepped down from 12 V to 6 V. During this disturbance, the voltage dropped to 36 V, and the controller required 13 ms to reach stability. The proposed ISMC does not result in any oscillations in the output voltage, as is evident in **Figures 14(c)** and **15(c)**. Similar observations can be made by examining the duty cycle (control input) shown in **Figure 16(c)**. This proves the validity and robustness of the proposed ISMC performance, despite the severity of the applied disturbance.

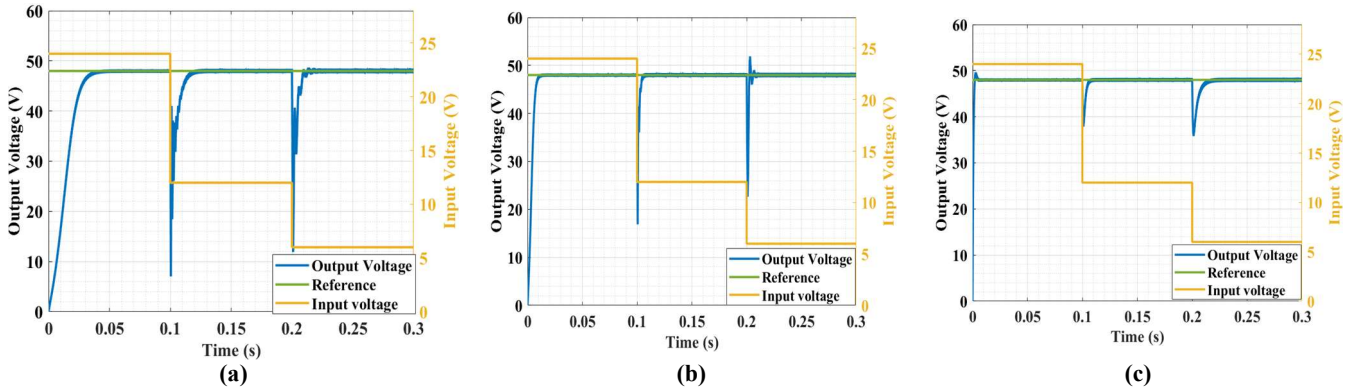


Figure 14. Second step change in the input voltage from 12 V to 6 V at $t = 0.2$s, and the corresponding output voltages. **(a)** Type-II compensator; **(b)** integral LQR; **(c)** proposed ISMC.

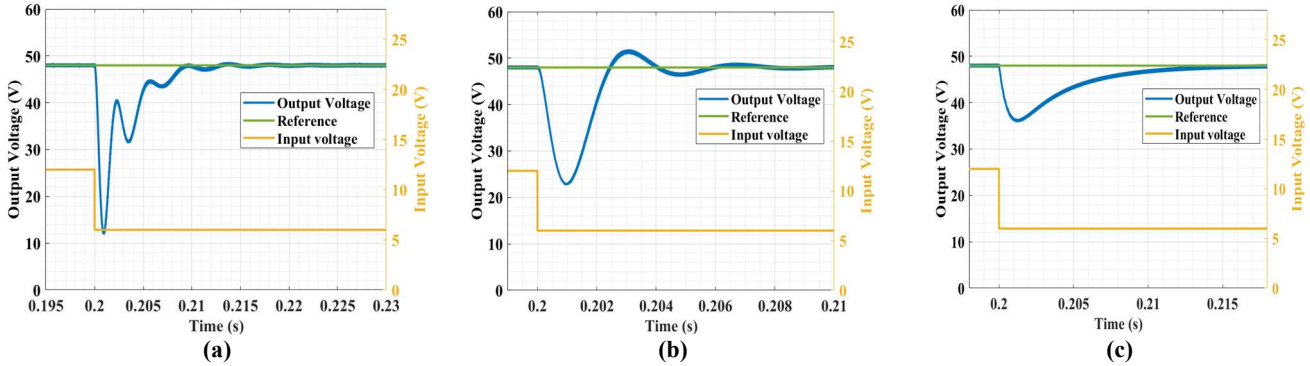


Figure 15. Zoomed portion of output voltage during the second disturbance at 0.2 s where input voltage changes from 12 V to 6 V. **(a)** Type-II compensator; **(b)** integral LQR; **(c)** proposed ISMC.

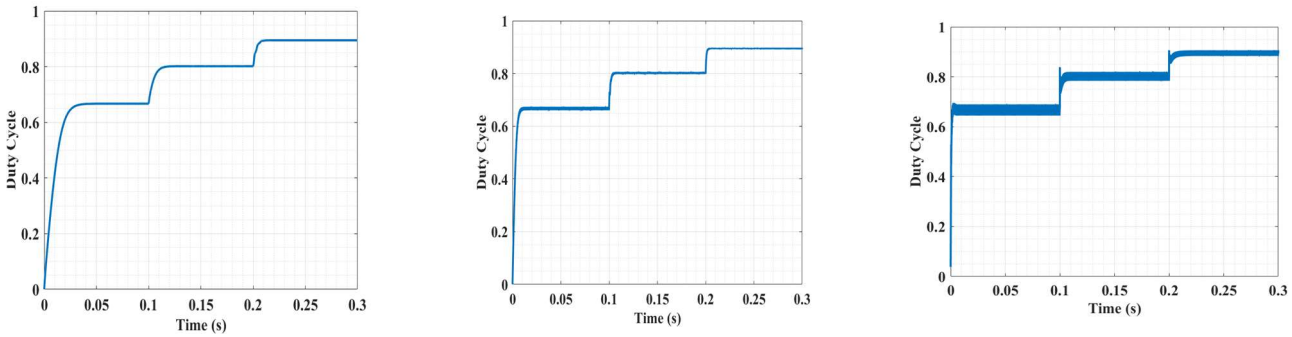


Figure 16. Controller duty cycles '*D*' throughout the different input voltage disturbances. **(a)** Type-II compensator; **(b)** integral LQR; **(c)** proposed ISMC.

In summary, this section covers the second test case, where the system was subjected to cascading severe disturbances in the input voltage. Studying the summary of results, as shown in **Table 5**, highlights the advantages of the proposed ISMC with respect to the other linear controllers. The results depicted in previous sections show that all the controllers can reject a disturbance in the input voltage up to 75% from the nominal state, which is 24 V. Although the proposed ISMC controller in this test is comparable to the Type-II compensator and relatively slower than the integral LQR controller, the ISMC controller offers other features that make it better than the discussed controllers. For instance, the output voltage dropped only to 36 V from 48 V due to the disturbance, while the voltage dropped to 22.5 V and 11.5 V in the case of the integral LQR and Type-II compensator, respectively. On a percentage basis, the 75% input voltage disturbance resulted in a deviation of 25%, 53%, and 76% for the ISMC, integral LQR, and Type-II compensators, respectively. This shows the significant advantage of the proposed ISMC.

Another point to highlight for the proposed ISMC is that the output voltage returns to the steady state after the disturbance in an oscillation-free response, unlike the case of the other linear compensators. This point is crucial in applications where fluctuations on the voltage rail can impact other sub-systems in the entire system. For instance, if the converter output is an input stage to another converter (such as motor inverters), then fluctuations in the first stage DC-DC converter output rail may disturb the second stage. Nevertheless, the proposed ISMC controller offers a smooth response for such cases where the input voltage may be disturbed by 75%. Furthermore, for this disturbance, the ripple in the output voltage does not have a noticeable increase after the disturbance is applied. This is categorized as a prime success in the design where the chattering is minimal, although the input disturbance is as high as 75%.

Table 5. Comparison of simulation results for input voltage disturbance.

Input voltage disturbance test			
	Type-II	**Integral LQR**	**Proposed ISMC**
Percentage change in input voltage	75%	75%	75%
Peak drop in output voltage	11.5 V	22.5 V	36.0 V

Table 5. (*Continued*).

Input voltage disturbance test			
	Type-II	**Integral LQR**	**Proposed ISMC**
Oscillations in response	Yes-severe	Yes-moderate	No
Settling time	15 ms	7 ms	13 ms

Load disturbance test:

The goal of this test is to investigate the converter response following a load disturbance. In this test, the converter will be subjected to 100% load variation to assess the controller's response under extreme conditions. The test demonstrates a severe condition as the load is varied by 100%, which results in doubling the delivered load current. During this test, the input voltage is kept constant at 24 V. After that, the load was varied by 100%, and the load resistance was dropped from 46 **Ω** to 23 **Ω**. This resulted in the delivered current increasing from 1.04 A to 2.08 A.

a) Using a type II compensator, the test resulted in oscillatory behaviour in the output voltage. The response shows an overshoot peaking at 52.5 V, followed by an undershoot peaking at 41 V. The transient in this test took 3.5 ms to settle and reach steady-state. Like the previous tests, the oscillatory behaviour is high and not desired in the response. **Figure 17(a)** shows the output voltage response under this load disturbance, and **Figure 18(a)** shows a zoomed capture of this response.

b) Simulating an integral LQR controller resulted in the results that are shown in **Figure 17(b)**. Analysing the depicted results shows that the test resulted in oscillatory behaviour in the output voltage. The response shows an overshoot that is contained within the 2% settling time criteria, followed by an undershoot that peaked at 41 V. The transient in this test took 2.5 ms to reach steady-state. Like the previous tests, the oscillatory behaviour is high, and it is not desired in the response. **Figure 18(b)** shows a zoomed capture of this response.

c) The proposed ISMC controller was tested for this case. The output voltage response under this test is shown in **Figure 17(c)**. Studying the results in **Figure 17(c)** concludes that the proposed controller can reject extreme variation in the load as a disturbance. The response has no oscillation, despite the significant change in the load. The designed controller was able to reject the disturbance in 6 ms, and the peak during the transient process reached 36 V. Furthermore, the compensator was able to reject the disturbance without compromising the output voltage ripple, unlike the case with linear compensators. The smooth response and low ripple system are desired features in the power converter field that the proposed ISMC can offer, unlike the discussed linear compensators. **Figure 18(c)** shows a zoomed capture of this response.

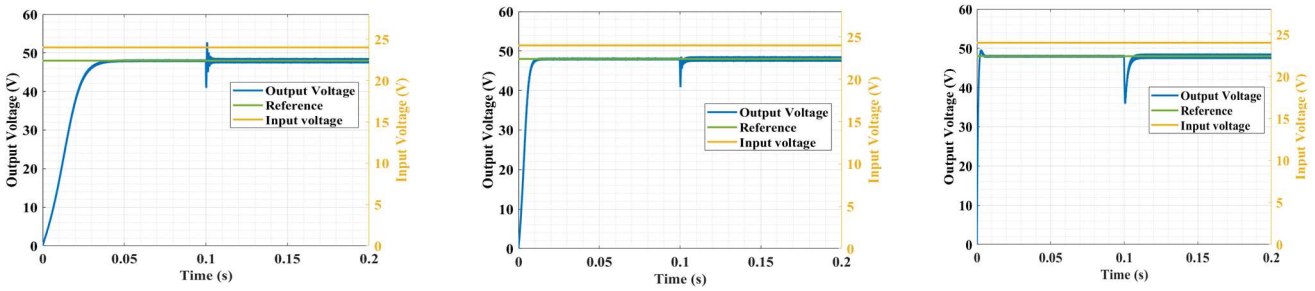


Figure 17. Output voltage at case 4: **(a)** Type-II; **(b)** integral LQR; **(c)** proposed ISMC.

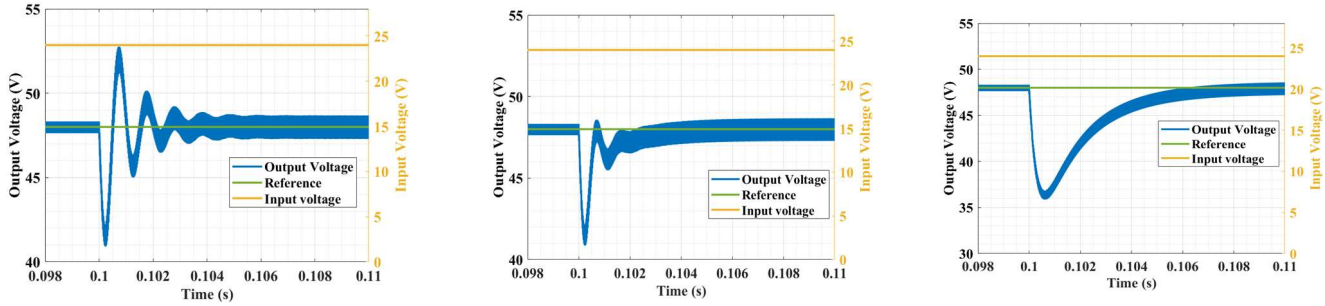


Figure 18. Zoomed portion of the output voltage at case 4: **(a)** Type-II; **(b)** integral LQR; **(c)** proposed ISMC.

In summary, this sub-section shows the results of testing the system against load disturbances. This is to investigate how well the compensator can operate under severe conditions. The following analysis focuses on the fourth stage. A summary of the results is highlighted in **Table 6**. Analyzing the obtained results as per **Table 6** concludes that in terms of the undershoot, once the load is changed from 46 to 23 **Ω**, both linear controllers are comparable, as the voltage dropped to 41 V while using the proposed ISMC, the voltage dropped to 36 V. From the settling time perspective, the linear controllers required 3.5 ms and 2.5 ms for Type-II and integral LQR controllers, respectively. The proposed ISMC required around 6 ms to recover from the transient. The key point and the advantage that the controller is bringing to the discussion is its ability to reject the disturbance in a response that is oscillation-free. Type-II and integral LQR controllers were able to reject the disturbance faster than the proposed ISMC; however, both linear controllers suffered from oscillations during the recovery process, and this would make the response unacceptable in the power electronics field. This is because having an oscillation may impact the performance of other stages and may drive the system out of stability if the other stages are not designed to tolerate such oscillations in the response. It should be noted that the output voltage did not suffer from high chattering using the ISMC. This is evident from analysing the ripple of the output voltage, where the maximum ripple did not exceed 2 V under 100% load variation. As discussed, this outstanding outcome is a result of the proper design of the sliding surface, proper selection of $\boldsymbol{\lambda}$ term, and selecting the system to operate on a PWM fixed frequency.

Table 6. Comparison of simulation results for load disturbance-derated system.

Load disturbance test 46–23 Ω			
	Type-II	**Integral LQR**	**Proposed ISMC**
Load variation	100%	100%	100%
Peak drop in output voltage	41 V	41 V	36 V
Oscillations in response	Yes-severe	Yes-moderate	No
Settling time	3.5 ms	2.5 ms	6 ms

7.2. Experimental results: Derated system: Type-II and proposed Controllers

In this section, the experimental work on the designed converter was conducted at derated power of 24 W, where the load was changed to 24 Ohm. The experimental work used the components summarized in **Table 7**. Following the simulation testing plan, the experimental work will be conducted under the same tests and conditions. In other words, this section will investigate the designed Type-II compensator as well as the proposed ISMC experimentally. Within all the next tests, Type-II compensator is $G_{comp} = \frac{5392.20s+685773\ .57}{3337.37s^2+6857734.57s}$, while for the proposed controller, the Lambda (λ) is set at 400.

Case 1: Cold start test:

In this case, the converter using the controller of interest is tested experimentally where it starts from rest and all the initial conditions are zero.

Table 7. Component list to conduct the experimental work.

Components	**Part number**
SEPIC converter	As developed in **Table 1**
Main power supply	ITECH—IT6006C-500-40
Auxiliary power supply	KORAD KA6003P
Oscilloscope	ROHDE & SCHWARZ RTB2004
Differential probe	CAL Test—CT3683
Voltage probe	ROHDE & SCHWARZ RT-ZP10
Microcontroller	Texas Instruments LAUNCHXL-F28069M

The test outcomes are summarized in the following points:

a) For the Type-II compensator, the output voltage response is shown in **Figure 19**. The figure shows the output voltage, and the horizontal and vertical divisions are 5 V and 20 ms, respectively. Analyzing the results in **Figure 19** highlights the following facts: The output voltage response is overdamped, and no oscillations are observed during the transitions. Having an overdamped response is a highly desirable feature in a power converter; nevertheless, the response took 70.7 ms to reach the steady state. Furthermore, the steady-state value of the output voltage is 23.3 V, which corresponds to a 2.91% steady-state error.

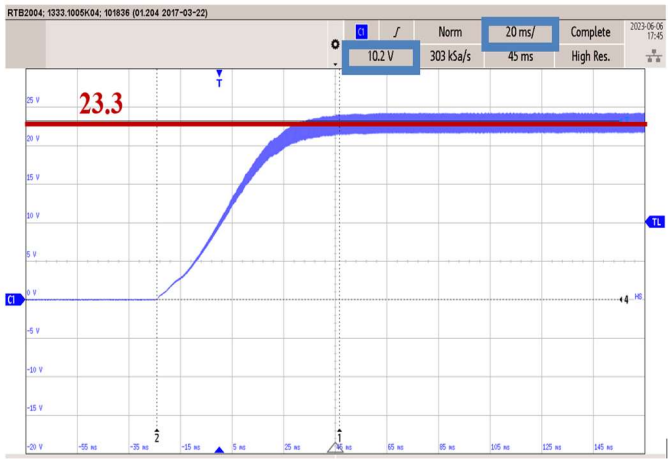


Figure 19. Voltage response for the de-rated power scenario using Type-II compensator-experimental result.

The required time to reach steady-state with respect to switching frequency is relatively extremely high and not desirable although the response is overdamped.

b) For the proposed ISMC, the output voltage response is shown in **Figure 20**. The figure shows the output voltage, and the horizontal and vertical divisions are 10 V and 2 ms, respectively. Studying the results in **Figure 20** shows the output voltage response has an overshoot that reaches 29 V with a settling time of 5 ms, with no other oscillations observed during the transitions. The response is very close to an overdamped response, which is desirable in a power converter, as well as being much faster than Type-II compensators. The steady-state voltage is at 25 V, which translates to 4.17% steady-state error, which is less than 5% acceptance criterion.

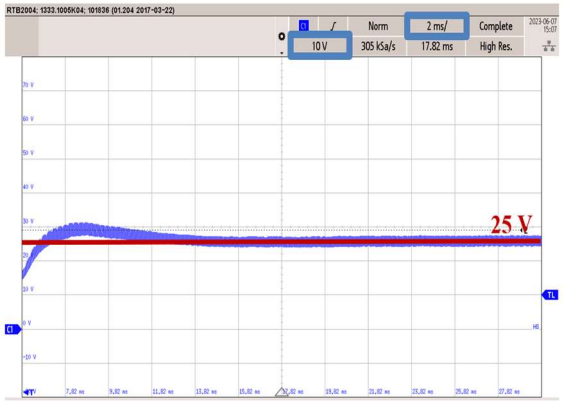


Figure 20. Voltage response for the de-rated power scenario using proposed ISMC-experimental result.

In summary, the cold start is implemented by turning on the system from rest and then waiting for the system to reach steady state. The main challenge in this test is starting from zero initial conditions (i.e., charging the storage elements of the SEPIC converter is becoming part of the picture where their status is starting from zero). **Table 8** summarizes the results of the experimental cold start test using the Type-II compensator vs. the proposed ISMC controller.

Table 8. Comparison of experimental results for cold test- derated system.

Cold start test		
	Type-II	**Proposed ISMC**
Response	Overdamped	Underdamped-close to critical damped
Settling time	70.7 ms	5 ms

The summarized results state that the linear compensator, Type-II compensator, has an overdamped response, and it took 70.7 ms to reach the steady state. On the other hand, the proposed controller was much faster, although there was a minor overshoot in the output voltage response. Specifically, the proposed ISMC controller required 5 ms to reach steady and this is approximately 14 times faster than the classical linear controller. During the test, the overshoot has reached 29 V, given that the reference is the step function. Ideally, an overshoot may not be a desirable feature in the power converters; however, in power electronics field, the reference is provided typically in a ramp function format to eliminate such overshoots that appear if the reference is a step function. Moreover, the proposed ISMC controller can be tuned easily by readjusting the λ value. Hence, if the goal is to achieve a cold start using the step function without an overshoot, then the designer can reduce the used λ value accordingly until the desired response is achieved.

Studying the depicted results of the cold start test results in observing that the output voltage from the proposed controller has a low ripple, around 2 V (pp), which is like the linear case. Sliding mode controllers usually suffer from a chattering in the output response if a sign function is used as part of the controller. This result emphasises the contribution of this work, as the design procedure is based on understanding and analyzing the relationship between the converter states on the novel constructed surface. Furthermore, the scaling constant, λ term, has been bound in this work to ensure system stability with lower chattering behaviour. Another point to highlight, is the selection of operating the system on a fixed frequency has a contribution to reducing the chattering as the converter internally is seeing an equivalent DC value of the duty cycle; this makes the converter operate in PWM mode, which effectively and inherently results in a low ripple system if the converter components are well sized and selected.

Case 2: Input voltage disturbance test:

After reaching steady-state, the input voltage is step changed from 12 V to 5 V (i.e., 58.3% disturbance). The results of this test are presented next:

a) Using the Type-II compensator, the output voltage response (**Figure 21**) shows the output voltage (in blue) as well as the input voltage (in magenta). The input voltage is stepped down to 5 V because, as confirmed by the simulation environment, 5 V is the lowest input that the compensator can tolerate to output 24 V while the power is at 24 W. Investigating the depicted results shown in **Figure 21** shows that the output voltage exhibited very minor oscillations during the transient process. Further, the output voltage dropped from 24 V to 8 V, where the settling time is around 25 ms. It should be noted that there was a minor tracking error before and after the test. Before applying the voltage disturbance, the output voltage at steady-state was 23.3 V (2.91% error), while after the test,

the steady-state value became 24.8 V (3.33%).

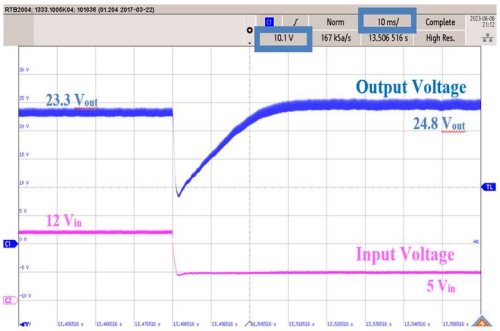


Figure 21. Voltage response for the de-rated power scenario using Type-II compensator-experimental result for input voltage disturbance.

b) Using the proposed ISMC, the input voltage is stepped down from 12 V to 3.5 V, which is equivalent to a 70.8% disturbance from the nominal input voltage. The corresponding results of this test in terms of output voltage response are shown in **Figure 22**. The figure shows the output voltage as well as the input voltage in blue and magenta traces, respectively. The vertical divisions for both measurements are in 10 V, while for the time scale, the divisions are in 5 ms. In this test, the input voltage was reduced to 3.5 V. The input voltage has been stepped down to 3.5 V because this is the lowest input that the compensator can tolerate to output 24 V at a 24 W load size. Therefore, stepping down the input voltage to 3.5 V is the maximum extreme condition that the system can be subjected to and tested against. Investigating the depicted results shown in **Figure 22** shows that the output voltage does not exhibit any oscillations during the transient process. Also, at the time of the disturbance, where the input voltage changed to 3.5 V, the output voltage dropped to 10 V, and it took 8 ms to recover from this disturbance. The obtained output voltage profile is highly favorable in the field of power electronics as the waveforms do not have any oscillations, yet it is fast enough compared to linear compensators. In terms of steady-state error, the output voltage after the disturbance was 24.4 V, which is equivalent to 1.67%.

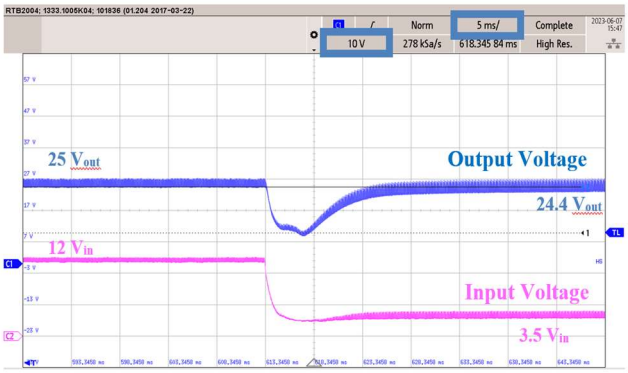


Figure 22. Voltage response for the de-rated power scenario using proposed ISMC-experimental result for input voltage disturbance.

In a nutshell, the system was tested against a severe change in the input voltage in the form of a step disturbance. Studying the summary of the results as shown in

Table 9 highlights the added advantages of the proposed ISMC. Although both controllers were capable of rejecting the introduced step input voltage disturbance, the proposed ISMC figures exceed the performance of the benchmark design Type-II compensator. Experimentally, the proposed ISMC can reject a disturbance up to 70.8% of the nominal input voltage, unlike the linear controller, which can handle up to 58.3% of the of the disturbance. Moreover, the ISMC controller was capable of handling the disturbance better than the linear compensator; this is evident in the output voltage, as the voltage dropped to 10 V in the ISMC case while the output voltage dropped to 8 V in the Type-II compensator case. The time that it took the controller to overcome the disturbance is another factor in comparing the designs. The results in **Table 9** show that the proposed controller is capable of rejecting a 70.8% disturbance in input voltage in 8 ms, which is around 3 times faster than a Type-II compensator. It should be emphasised on the fact that the output voltage in the case of the ISMC controller returns to the steady state after the disturbance introduction in a smooth oscillation-free response, unlike the case of the linear compensator. This point is crucial in applications where fluctuations on the voltage rail can impact the other sub-systems of the entire system. For instance, if the output of the converter is an input stage to other converters, such as motor inverters, then fluctuations on the converter output rail may disturb the second stage, and other considerations should be investigated. Nevertheless, the proposed ISMC controller offers a fast and smooth response in such cases where the input voltage is disturbed. Furthermore, for a disturbance of 70.8% in the input voltage, the ripple has increased to be around 3.75 V from 2 V, which is classified as prime success in the design where the chattering is minimal, although the disturbance was about 70.8% from the nominal case.

Table 9. Comparison of simulation results for input voltage disturbance- derated system.

Input voltage disturbance test		
	Type-II compensator	**Proposed ISMC**
Lowest input voltage	5 V	3.5 V
Max percentage of change	58.30%	70.8%
Peak undershoot in output voltage	8 V	10 V
Oscillations in response	Yes-minor	No
Settling time	25 ms	8 ms

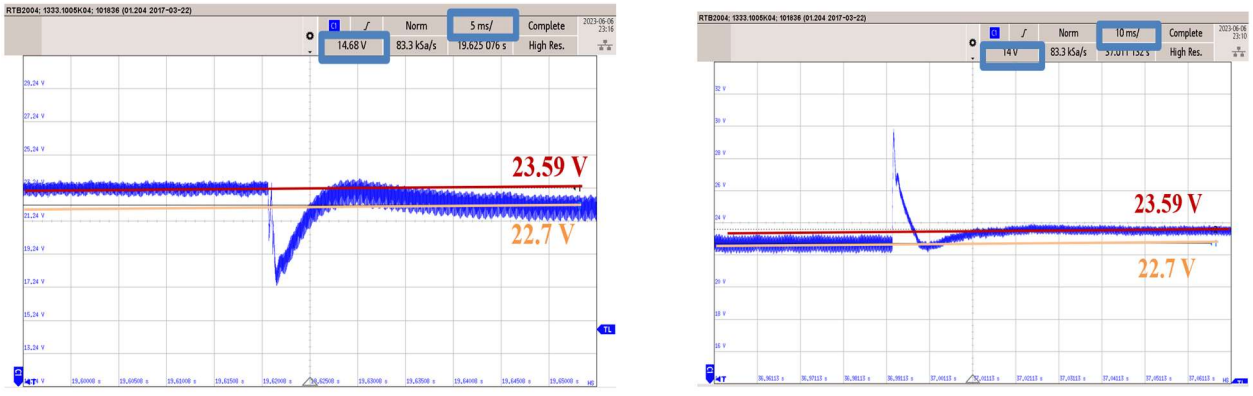
Case 3: Load disturbance test:

In this case, the system is investigated to reject 100% load disturbance. The test procedure will be started by running the converter at a cold start until the output voltage reaches the desired level of 24 V. After that, the load will be changed by 100%, i.e., the impedance will be changed to 12 Ω. Next, the load will be returned to its nominal condition, where the load will be changed from 12 Ω to 24 Ω. The results of the described test are presented next:

a) The zoomed portion of the output voltage response using Type-II is shown in **Figure 23(a,b)**. In both zoomed portions, the figures show the output voltage, while the vertical and horizontal divisions are 14.68 V and 5 ms for the first and

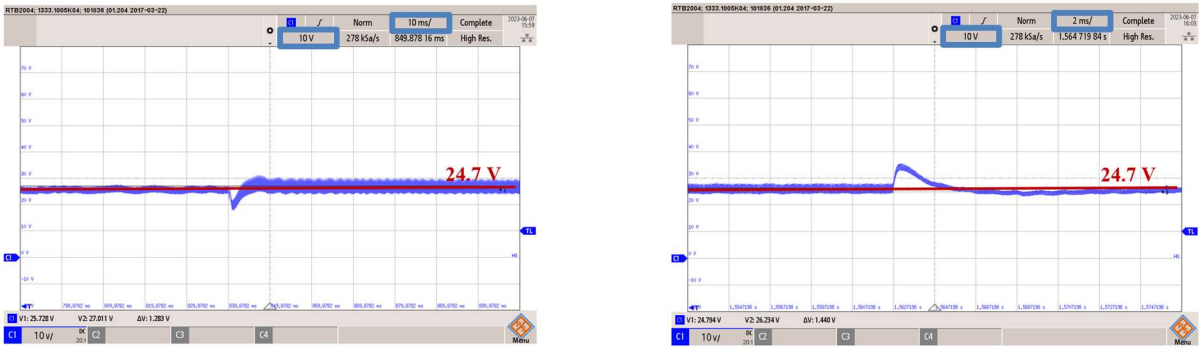
14 V and 10 ms for the second. In the first disturbance scenario, where the load is changed from 24 Ω to 12 Ω, the output voltage displayed oscillations that started with an undershoot that peaked at 17.4 V. The process of recovery from the first disturbance took 20 ms. At the second disturbance, a similar response was obtained, where the response suffered from oscillations that peaked at 30 V. The system took 20 ms to reject the disturbance and return to steady-state. Another observation to note is the level of steady-state voltage before and after the disturbance. Before the first disturbance, the output voltage was 23.3 V, then dropped to 22.7 V after the disturbance; furthermore, it should be noted that after the first disturbance, the ripple increased, which is an expected outcome due to the extreme loading condition. After the second disturbance, where the load changed from 12 Ω to 24 Ω, the output voltage steady-state value changed from 22.7 V to 23.6 V.

b) The proposed ISMC controller resulted in the responses depicted in **Figure 24(a,b)** (zoomed portion). In both zoomed portions, the figures show the output voltage, while the vertical divisions are 10 V. The horizontal divisions are 10 ms and 2 ms for the first and second scenarios, respectively. Studying these responses results in the next observation. In the first disturbance scenario, where the load is changed from 24 Ω to 12 Ω, the output voltage did not have any oscillations in the transients. The response has an undershoot that peaked at 19.6 V, then it reached the steady-state again in a smooth response. The process of recovery from this disturbance took 2 ms. At the second disturbance, a similar response was obtained, where the output voltage had a smooth recovery during the transients. Specifically, the transients started with an overshoot that peaked at 33.6 V, then the output voltage recovered in a smooth response. In this case, the system took 3 ms to reject the disturbance and return to steady-state level. Studying the results shows that the ripple increased after the first disturbance, and this is expected due to the significant loading condition, like in the case of the linear compensator. Another point that should be noted is that after the disturbance, the output voltage at steady-state was 24.7 V, which confirms the design was successful.



(a) **(b)**

Figure 23. Zoomed portion at voltage response for the de-rated power scenario using Type-II compensator-experimental result for load disturbance from **(a)** 24 Ω to 12 Ω; **(b)** 12 Ω to 24 Ω.



(a) **(b)**

Figure 24. Zoomed portion at voltage response for the de-rated power scenario using proposed ISMC-experimental result for load disturbance from **(a)** 24 Ω to 12 Ω; **(b)** 12 Ω to 24 Ω.

In short, the system was tested against 100% load variation where this test aimed to investigate how well the compensator is capable of operating under severe conditions. A summary of the presented results in the previous subsections under this test case is highlighted in **Table 10**. Analyzing the obtained results as per **Table 10**, it can be concluded that in terms of the undershoot, once the load is changed from 24 to 12 Ω, both controllers are comparable, with a slight advantage to the linear compensator as peak response. Similarly, once the load is changed again from 12 to 24 Ω, both controllers result in an overshoot with a minor advantage towards the linear compensator in terms of the maximum peak value. However, in terms of how smooth the response is, the proposed ISMC is taking the lead. As shown in the previous subsections, the proposed ISMC response does not have any oscillation, whether the load is changed from 24 to 12 Ω or vice versa. On the contrary, the linear compensator response showed an undershoot followed by an overshoot for the 24–12 Ω case and showed an overshoot cascading with an undershoot for the scenario of 12–24 Ω. Having a system with no oscillation sin the recovery process is a highly desirable feature in the power electronics field. This is because having an oscillation may impact the performance of other stages and may drive the system out of stability if the other stages are not designed to tolerate such oscillations in the response. From a settling time perspective, the proposed ISMC controller demonstrates a superior result experimentally. The proposed ISMC controller was capable of rejecting load disturbances 7–10 times faster than the Type-II compensator without having any oscillations in the response. From a power converter perspective, this result brings significant advantages to the field because the response is smooth without compromising the recovery time.

It should be noted that the output voltage in this test for both scenarios did not suffer from high chattering. This is evident through dissecting the ripple of the output voltage, where the maximum ripple did not exceed 5 V under 100% load variation while the ripple is maintained around 2 V whenever the load is back to 24 Ω. This is an outstanding result due to the proper construction of the sliding surface, the proper selection of λ term, and the selection of the system to be operating on a PWM fixed frequency structure.

Table 10. Comparison of simulation results for load disturbance- derated system.

Load disturbance test 24–12 Ω		
	Type-II compensator	**Proposed ISMC**
Load variation	100%	100%
Peak undershoot in output voltage	17.4 V	19.6 V
Oscillations in response	Yes-minor	No
Settling time	20 ms	2 ms
Load disturbance test 12–24 Ω		
	Type-II Compensator	**Proposed ISMC**
Load variation	100%	100%
Peak overshoot in output voltage	30 V	33.6 V
Oscillations in response	Yes-minor	No
Settling time	20 ms	3 ms

8. Conclusion

This work proposes a systematic approach to designing an integral sliding mode controller for a SEPIC converter. Furthermore, the work summarized the design guide for a Type-II compensator as well as an integral LQR where these controllers were compared to the proposed controller. The designed controllers were simulated in a Simulink environment using a switched converter model and then validated through a scaled experimental setup. The hardware results confirm the simulation results, and they show the benefits that can be achieved by designing and implementing the ISMC for SEPIC converter. As highlighted in the literature, one of the prime limitations of using the sliding mode controller in industry is the lack of a standardized approach to design the controller, and this issue was addressed in this work.

Author contributions: Conceptualization, YEH, VS and RM; methodology, YEH, VS; software, YEH; validation, YEH, VS and AS; formal analysis, YEH and VS; investigation, YEH and VS; resources, VS; data curation, YEH and VS; writing—original draft preparation, YEH, VS and AS; writing—review and editing, VS; visualization, YEH, VS and AS; supervision, VS and RM; project administration, VS; funding acquisition, VS. All authors have read and agreed to the published version of the manuscript.

Conflict of interest: The authors declare no conflict of interest.

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